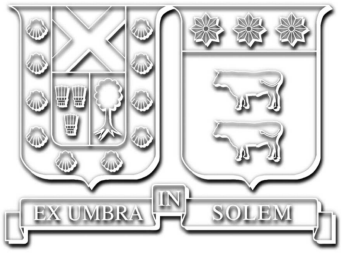
U. Técnica Federico Santa María - Technische Universität Berlin
Departamento de Ingeniería Electrónica - Faculty IV Power Electronics Department
Valparaíso, Chile - Berlin, Deutschland



UNIVERSIDAD TECNICA
FEDERICO SANTA MARIA

Design, Control and Analysis of a Novel Multilevel Converter with Reduced Switch Count

Margarita A. Norambuena Valdivia

2017

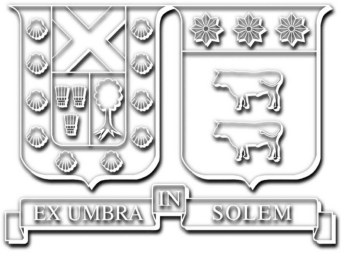
In partial fulfillment of the requirements for the grade of:
Doctor of Philosophy in Electronic Engineering (UTFSM)
Doktor der Ingenieurwissenschaften (TUB)

Thesis Supervisor:
Dr.-Ing. José Rodríguez Perez (UTFSM)
Dr.-Ing. Sibylle Dieckerhoff (TUB)

Thesis Examiner:
Dr. Samir Kouro Renaer (UTFSM)
Dr. Marcelo Pérez Leiva (UTFSM)
Dr.-Ing. Ralph Kennel (Technische Universität München)

Valparaiso, July, 2017.

U. Técnica Federico Santa María - Technische Universität Berlin
Departamento de Ingeniería Electrónica - Faculty IV Power Electronics Department
Valparaíso, Chile - Berlin, Deutschland



UNIVERSIDAD TECNICA
FEDERICO SANTA MARIA

Design, Control and Analysis of a Novel Multilevel Converter with Reduced Switch Count

Margarita A. Norambuena Valdivia

2017

“No tengo algún talento especial, sólo soy extremadamente curioso.”
,,Ich habe kein besonderes Talent, Ich bin nur sehr neugierig.“
— Albert Einstein

Acknowledgments

This PhD project has been done at the Chair of Industrial Electronics of Electronic Department at Universidad Técnica Feerico Santa María (UTFSM), Valparaíso, Chile and at the Chair of Research group of Power Electronics at Faculty IV - Electrical Engineering and Computer Science at Technische Universität Berlin (TUB), Berlin, Germany. The four years I have spent on this PhD have been very interesting and educational. I would never have been able to finish my PhD dissertation without the guidance of my supervisors.

Firstly, I would like to express my deepest gratitude to my supervisor Prof. Dr.-Ing. José Rodríguez for his constant guidance, helpful comments, advice, interest, and support. Prof. Rodríguez has been always giving me the confidence and security to think with freedom and to implement my new ideas. I am deeply happy to have him as my supervisor, he is a very interesting person, he always gave me some of his time when I needed it, and always available to talk, not only of my PhD work, also to talk about new tendencies in the world, the good music and the best place to go to visit.

I would like to express my deepest gratitude to my supervisor Prof. Dr.-Ing. Sibylle Dieckerhoff for accept me, for her interest, helpful comments, advice, and support. Prof. Dieckerhoff gave me the space, the opportunity and the trust to convert my ideas in reality. I cannot imagine being able to finish my PhD dissertation without her assistance and support. She is a very meticulous person, organized, clear in her goals and in the steps that must be followed and I admire her for that.

I would like to thank Prof. Dr. Samir Kouro for being the co-supervisor of my PhD dissertation from UTFSM. It was his comment about a new back-to-back two-level converter, the angular stone to made possible this PhD dissertation.

Besides my supervisors, I would like to thank Prof. Dr.-Ing. Ralph Kennel for being the fourth examiner for this dissertation.

My sincere thanks go to my colleagues in TUB and UTFSM, especially I would like to express my gratitude to Tino Kahl for his help and friendship during my stay in Berlin and after that. Tino has a wide knowledge and experiences on building PCBs and without his help and comments my work would have taken more time and probably I still would be trapped in beginner mistakes.

I would like to thank administrative and technical staff members of the chair at TUB who have been kind enough to advise and help in their respective roles. I thank Mrs. Gudrun Pourshirazi for her help, cooperation and time.

I would like to thank my parents, and siblings for supporting me spiritually throughout writing this dissertation and my life in general, even through the distance.

I am grateful to the support of the Chilean Research Council(CONICYT) under grant "Doctorado Nacional 2014" (21140574), FONDECYT under grant 1170167 and also the

support of German Academic Exchange Service (DAAD) under grant “Bi-nationally Supervised Doctoral Degrees” (57129430) for funding my PhD project period.

Y por último, agradezco a la persona más trascendental de mi vida, porque sin ella jamás hubiera podido llegar hasta donde estoy, mi Padre Dios es lo más importante que podría llegar a tener. Todo por él y nada sin él.

Table of Contents

Figures Index

Tables Index

Abstract

Multilevel converters are used in a wide range of applications, such as drives, energy conversion and distributed generation. This Thesis proposes a new multilevel converter topology that allows increasing the number of output voltage levels with a reduced number of necessary power semiconductors in comparison with standard multilevel topologies such as Active Neutral Point Clamped (ANPC), Flying Capacitor Converter (FCC) and Stacked Multicell Converter (SMC).

The proposed topology consists of a cascaded connection of basic units called *main cells*, which are composed of three power switches and one flying capacitor, and two output switches for each output phase.

In this Thesis, the comparison for the required number of power switches, voltage stress across the switches, power distribution, capacitors size and energy storage of the proposed topology with conventional topologies such as ANPC and SMC are discussed.

To verify the performance of the proposed multilevel topology, extensive simulations and experimental studies were carried out on a 3-phase 5-levels.

Resumen

Los convertidores de potencia multinivel son empleados en una amplia gama de aplicaciones, incluyendo: máquinas y accionamientos, conversión de energía y generación distribuida. Esta Tesis propone una nueva topología de convertidor multinivel que permite incrementar el número de niveles de tensiones a la salida del convertidor empleando un reducido número de semiconductores de potencia en comparación con topologías multinivel convencionales, tales como el convertidor Active Neutral Point Clamped (ANPC), el convertidor Flying Capacitor (FCC) y el convertidor Stacked Multicell (SMC).

Esta topología está conformada por la conexión en cascada de unidades básicas llamadas *celdas principales*, que se componen por un condensador flotante y tres semiconductores de potencia, y dos semiconductores de potencia para seleccionar la salida de tensión correspondiente a cada fase del sistema.

En este trabajo se discute el número de semiconductores de potencia requeridos, el estrés de tensión a los que son sometidos, la distribución de potencia a través de ellos y la energía almacenada en los condensadores flotantes en comparación con topologías estándares y comerciales como los son el ANPC y el SMC.

La validación de la topología multinivel propuesta es verificada a través de simulaciones y resultados experimentales en un prototipo trifásico de 5 niveles.

Kurzfassung

Mehrstufige Wechselrichter werden bei einer Vielzahl von Anwendungen eingesetzt: Als Treiber für elektrische Antriebe, für die Energieumwandlung oder für die Erzeugung verteilter Netze. Die vorliegende Arbeit beschreibt eine neuartige, mehrstufige Konverter-Topologie, die eine Erhöhung der Ausgangsspannungslevel ermöglicht. Im Vergleich zu Standard-Multilevel-Topologien, wie Active Neutral Point Clamped (ANPC), Flying Capacitor Converter (FCC) und Stacked Multicell Converter (SMC), werden gleichzeitig die notwendigen Leistungshalbleiter reduziert.

Die vorgeschlagene Topologie besteht aus einer Zweierverbindung Kaskadenschaltung der Basiseinheit, genannt ,,main cells“. Diese ,,main cells“ besteht aus drei Leistungsschaltern und einem ,,Flying capacitor“. Für die Ausgangsphasen werden Halbbrücken mit zwei Leistungsschaltern verwendet.

In dieser Arbeit wird der Vergleich für die erforderliche Anzahl von Leistungsschaltern, die Spannungsbelastung der Schalter, Leistungsverteilung, Kondensatorgröße und die gespeicherte Energie der vorgeschlagenen Topologie mit herkömmlichen Topologien − wie ANPC und SMC − diskutiert.

Um die Leistungsfähigkeit der vorgeschlagenen mehrstufigen Topologie zu validieren, wurden umfangreiche Simulationen und experimentelle Untersuchungen für 3-phasige 5-Level-Topologien durchgeführt.

Chapter 1

Introduction

Voltage source Converters (VSC) have today a wide variety of applications [1–3], such as:

- Industry: Pumps, ventilators, conveyors, mills, etc.
- Transportation: Trains, trucks, cars, airplane.
- Transmission and distribution of energy: wind farms, HVDC, STATCOMs, active filters, etc.
- Drives: Load side and grid side converter.

The VSC can behave as a rectifier (VSR-*Voltage Source Rectifier*) or as an inverter (VSI-*Voltage Source Inverter*) depending on the direction of the power flow. Therefore, it is a fully bidirectional structure.

Because of its simple structure and mature technology, the two-level VSC has been the most attractive option for the industries [4]. However, the two-level VSC provides a poor voltage quality. Large harmonic content of the output voltage of a two-level VSC hampers its application in supplying sensitive loads and also in grid-connected energy conversion systems where strict grid codes should be addressed. Adding harmonic filters to the output of a two-level VSC for improving the power quality results in a complex, expensive and bulky system which is less attractive for the industries.

Multilevel VSCs provide several voltage steps by which a more sinusoidal voltage waveform can be constructed. Multilevel converters have emerged as an attractive solution for power electronics applications due to numerous merits over classical two-level converters such as: better output voltage waveform quality, lower harmonic distortion of the input and output currents, reduced filter size, lower common-mode voltages, reduced electromagnetic interference, reduced torque ripple in drive applications and feasible fault tolerant operation [5].

Multilevel converters consist of an array of semiconductor devices and capacitive voltage sources, which can generate output voltage waveforms with multiple steps by appropriate switching. With the increase in the number of output voltage levels or steps, the staircase output waveform approaches a sinusoidal waveform.

The 3-level Neutral Point Clamped (NPC) converter is one of the classical multilevel topologies [6]. The NPC has become popular due to its simple structure, but it has not been extended to higher level operation due to excessive losses of clamping diodes, uneven distribution of losses in inner and outer devices and the need to balance the capacitor voltages [7].

The concept of multicell converters introduced 20 years ago allows an important advance in the domain of medium voltage (3kV, 4.5kV, 6.6kV) and high power (several MW) applications. The development of static converters dedicated for high power applications currently increase. By using series connection of commutation cells, it can easily increase the input voltage of converters and improve waveforms while using smaller components with better properties. The Flying Capacitor Converter (FCC) is an example of these topologies [8, 9].

The Stacked Multicell Converter (SMC) is a novel topology of multilevel converter in the same line of the flying capacitor converter and allows converters to reach output voltage, output power and performances still higher than the classical multicell converter FCC [10].

The SMC like the FCC use flying capacitors and the voltage across these flying capacitors have to be balanced to allow for a correct operation of multicell topologies. When Pulse Wide Modulation (PWM) techniques are used, it is necessary to study natural balancing properties of the SMC converter, and when Model Predictive Control (MPC) is used, it is possible to control directly these internal voltages. Some external circuits (such as RLC filter), can be used to increase the dynamic of the voltage balancing.

Multilevel converters are a good candidate for supplying sensitive loads and being used in the grid-tied system, due to their good power quality, higher efficiency and better electromagnetic compatibility (EMC) [11, 12]. Different structures of multilevel converters have been reported in the literature in the last years. This thesis proposes a new multilevel converter structure which reduces the necessary number of power switches and flying capacitors to generate the same number of output levels than in classical topologies such as FCC, SMC and NPC.

The new multilevel topology is called Reduced Multilevel Converter (RMC), consists of a cascaded connection of basic units called main cells (MC) and 3-phase output inverter stage. The RMC is a multilevel inverter with a single DC-bus configuration. Every MC is formed by three power switches and one capacitor. The MCs works as a DC-DC multilevel converter, generating a variable *dc-link* in the output of the MCs. The output inverter stage can be any inverter with a single DC-bus configuration like the 2L-VSI, Neutral Point Clamped (NPC), ANPC, T-type [13], FCC, Stacked Multicell Converter. However, in this work, the basic 2L-VSI is used to be able to identify the real contribution of the RMC.

The upcoming chapters of this dissertation are organized as follow:

Chapter 2 presents a brief description of main multilevel converter with a single DC-bus configuration which will be used to compared the performance of the RMC. These topologies are: Neutral Point Clamped (NPC) converter, 5-level Active Neutral Point Clamped (5L-ANPC) converter, Flying Capacitor Converter (FCC) and Stacked Multicell Converter (SMC).

Chapter 3 presents the description of the proposed topology in this dissertation, the

Reduced Multilevel Converter, its basic properties, operation principle and mathematical model.

Chapter 4 gives a brief summary of Model Predictive Control (MPC), the control strategy used to control the proposed topology. This chapter describes the principal advantage and disadvantages of MPC strategy and its implementation scheme.

Chapter 5 presents a simulation analysis of the proposed topology compared with the multilevel converter described in chapter 2. The analysis is made considering the system answer, i.e. output currents, output voltages, capacitor voltage balance, harmonic spectrum, total harmonic distortion and dynamic characteristic, and the characteristics of the structure, i.e. blocking voltage, switching frequency, switching and conduction losses, storage energy and size of the inner capacitors.

Chapter 6 presents a experimental validation of the designed topology using a 5L-RMC prototype.

Finally, chapter 7 provides a brief summary of the whole dissertation and discusses some extended ideas that can be carried out in the future.

Chapter 2

Multilevel Converters

For power electronic applications, multilevel inverters are today a well accepted and mature technology. In this work, the following types of multilevel inverters will be considered:

Neutral Point Clamped (NPC) converter: A three-level NPC converter will be considered as the startup point to understand multilevel converters.

Active Neutral Point Clamped (ANPC) converter: A five-level ANPC converter will be considered as a comparison point for 5-level commercial topologies.

Flying Capacitor Converter (FCC): A FCC will be considered as the classical flying capacitor topology.

Stacked Multicell Converter (SMC): A SMC will be discussed as a flying capacitor commercial topology.

2.1. Neutral Point Clamped (NPC) Converter

The NPC converter was introduced in the early 1980s [6]. Today, the NPC topology has become very popular in industry and academic research all over the world. Some commercial examples are ACS1000 (ABB), MV Simovert (Siemens), TMdrive-70 (TMEIC-GE), Silcovert-TN (Ansaldo), MV7000 (Converteam) and IngeDrive MV500 (IngeTeam). The NPC inverters can be found in industry using IGCT (Integrated Gate Commutated Thyristor), IEGT (Injection Enhanced Gate Transistor), and medium-voltage IGBT (Insolated Gate Bipolar Transistor).

2.1.1. The power circuit

Fig 2.1 presents the power circuit of this topology. Each phase of the inverter has four power switches, composed by a power transistor with an antiparallel diode. In addition, two clamping diodes (D_{1x}, D_{2x}, $x \in \{a, b, c\}$) are used to connect the output terminal to the medium point (N) of the *dc-link* capacitors. This configuration allows to generate three voltage levels at the output terminal of phase x with respect to the neutral point

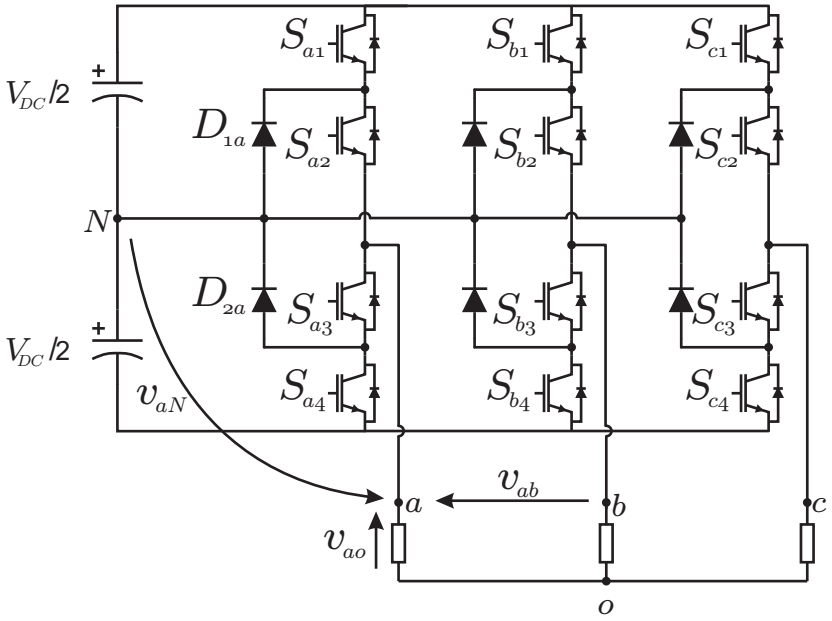


Figure 2.1. *Three Phase Inverter 3-level NPC.*

Table 2.1
Switching states for one phase of the NPC inverter

Switching State $(S_{x1}, S_{x2}, S_{x3}, S_{x4})$	**Output Voltage** v_{xN}
(1,1,0,0)	$V_{DC}/2$
(0,1,1,0)	0
(0,0,1,1)	$-V_{DC}/2$

N, considering the switching combinations given in Table 2.1. Where $S_{xi} = 0$ means that the power switch S_{xi} is OFF and $S_{xi} = 1$ implies that the power switch is ON, for all $i \in \{1, 2, 3, 4\}$.

Fig. 2.2 shows the levels of voltages generated at the NPC inverter output. The main parameters for the simulation setup are $V_{DC} = 200V$ and carrier PWM period $T_c = 1ms$. Since NPC has three levels between output terminal and neutral point of the inverter (v_{xN}), it will have $k = 2m - 1$ levels in the line to line voltages (v_{ab}), with m the number of levels at the output of inverter (v_{xN}). So, the voltage v_{xo} will have $2k - 1$ levels.

2.1.2. Vectors generated by the inverter

For the three phase inverter, 27 switching states are generated. Each switching state is represented by three possible values denoted by +, 0 and − that represent the switching combinations that generate $V_{DC}/2$, 0, and $-V_{DC}/2$ respectively, at the output of the inverter phase.

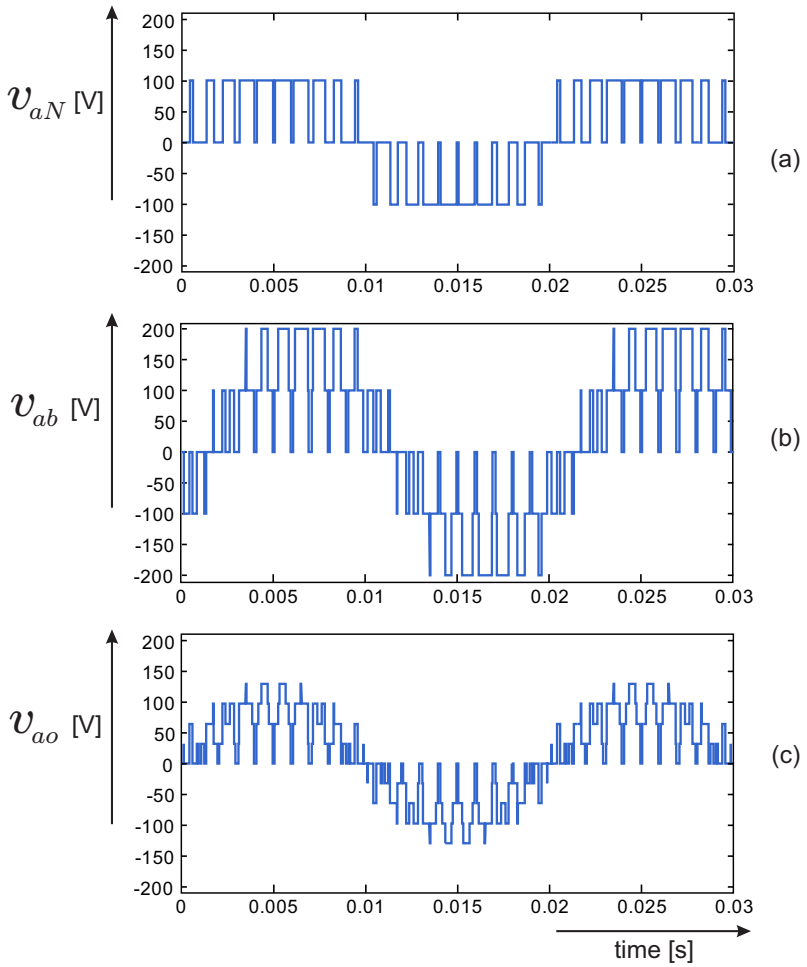


Figure 2.2. *NPC inverter output: (a) Voltage v_{aN}; (b) Voltage v_{ab}; (c) Voltage v_{ao}.*

Considering the space vector is defined for the output voltage:

$$\mathbf{v}_s = \frac{2}{3}[v_{aN}(t) + av_{bN}(t) + a^2 v_{cN}(t)] \tag{2.1}$$

$$a = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \tag{2.2}$$

$$a^2 = e^{j\frac{4\pi}{3}} = -\frac{1}{2} - j\frac{\sqrt{3}}{2} \tag{2.3}$$

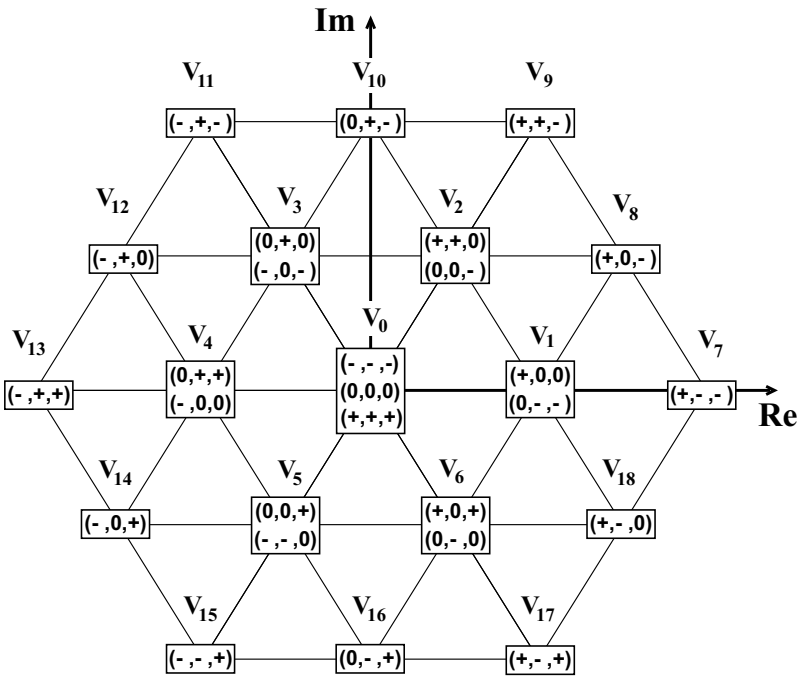


Figure 2.3. *Space vectors of NPC.*

And the definition of voltage states is described by:

$$S = (S_a, S_b, S_c) \tag{2.4}$$

$$S_{a,b,c} \in \{+, 0, -\} \tag{2.5}$$

$$\begin{aligned} \text{State } + &\rightarrow S_{x1}, S_{x2} \text{ are on} \\ \text{State } 0 &\rightarrow S_{x2}, S_{x3} \text{ are on} \\ \text{State - } &\rightarrow S_{x3}, S_{x4} \text{ are on} \\ \text{for } x &= a, b, c \end{aligned}$$

The 27 switching states produce 19 different voltage vectors, as shown in Fig. 2.3. Some switching states are redundant, generating the same voltage vector. For example, vector $\mathbf{V}_0$ can be generated by three different switching states: (+,+,+), (0,0,0), and (-,-,-).

$$\mathbf{V}_0 = \frac{2}{3}\left[\frac{V_{DC}}{2} + a\frac{V_{DC}}{2} + a^2\frac{V_{DC}}{2}\right] \tag{2.6}$$

$$\mathbf{V}_0 = \frac{2}{3}\left[0 + a0 + a^2 0\right] \tag{2.7}$$

$$\mathbf{V}_0 = \frac{2}{3}\left[\frac{-V_{DC}}{2} + a\frac{-V_{DC}}{2} + a^2\frac{-V_{DC}}{2}\right] \tag{2.8}$$

Voltage vectors $\mathbf{V}_1$ to $\mathbf{V}_6$ can be generated by two different switching states, that is, they present redundant switching states.

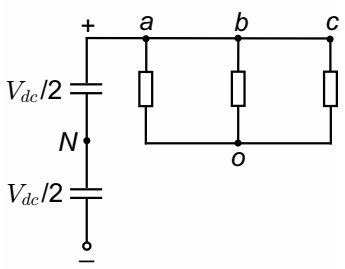


Figure 2.4. *Switching state for* $\mathbf{V}_0$. $S = \{+, +, +\}$.

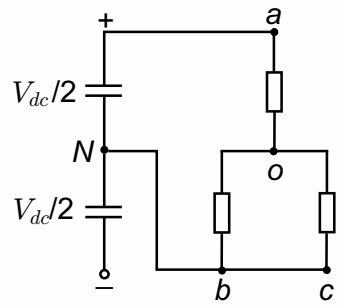


Figure 2.5. *Switching state for* $\mathbf{V}_1$. $S = \{+, 0, 0\}$.

Fig. 2.4 shows the configuration of the load considering a passive load (resistors) for switching a state vector $\mathbf{V}_0$, being $S = \{+, +, +\}$, and Fig. 2.5 shows the configuration for switching a state vector $\mathbf{V}_1$, being $S = \{+, 0, 0\}$.

2.1.3. The classical modulation

The classic PWM modulation is a special technique called: *Level Shifted PWM*. The LS-PWM used in this work consists of an Alternate Opposition Disposition [14].

Fig 2.6 shows the block diagram for connecting the signals to the power switches using a LS-PWM modulation, while Fig. 2.7 shows the waveforms for the classic LS-PWM modulation.

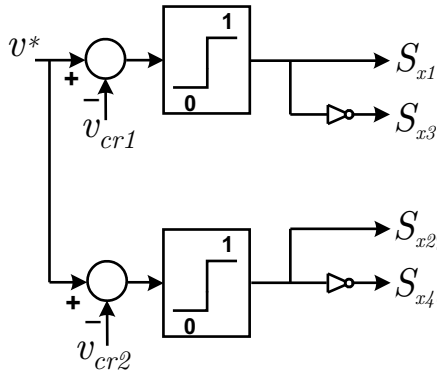


Figure 2.6. *Block diagram of Level Shifted-PWM modulation.*

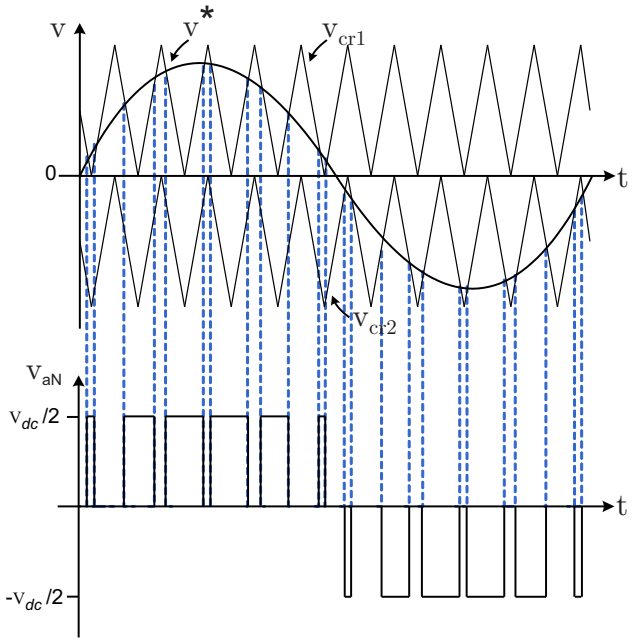


Figure 2.7. *Classic Level Shifted-PWM modulation.*

2.1.4. Summary

The main advantages and disadvantages of this topology can be summarized as follows.

Advantages :

- As a widely used topology, you can find enough information in the literature on its applications [14–18]. This means that the NPC is a mature technology, which is a decisive point to establish a new technology in the industry.
- It only needs one source of DC voltage to power all the inverter. The midpoints can be obtained using capacitors.

Disadvantages :

- Unequal distribution of losses between the inner and outer switching devices in each converter leg.
- Increasing number of clamping diodes are needed for higher number of levels.
- Depending on how the *dc-link* voltage, V_{DC}, is obtained, imbalances may arise between the capacitors. This drawback can be mitigated by modifying the control strategy [19–21].
- At higher number of levels, it is a problem to maintain the proper balance of voltage in capacitors. Therefore, the control law becomes more complex [22–26].

2.2. Active Neutral Point Clamped (ANPC) Converter

The design of the multilevel converters allows achieving several output levels. However, such circuits often come at the price of far higher complexity. For example, to generate 5 output voltage levels in the NPC it is necessary to use additional clamping diodes, capacitors and the corresponding control and charging circuitry, which is a complex control strategy, and even, more complex control might not be sufficient to operate an NPC with more than 3 levels. An alternative approach is to connect converters in series. This again adds to the complexity of the *dc-link* supply circuit due to the need for galvanic separation of the supplies and thus costly transformers [27, 28].

This issue can be solved by the 5-level ANPC that incorporates an additional capacitor per output phase. ABB commercializes the 5L-ANPC with his model ACS 2000.

2.2.1. The power circuit

Fig. 2.8 presents the power circuit of this topology. Each phase of the inverter has one capacitor and eight power switches, two of them are used to connect the medium point (N) of the *dc-link* capacitors.

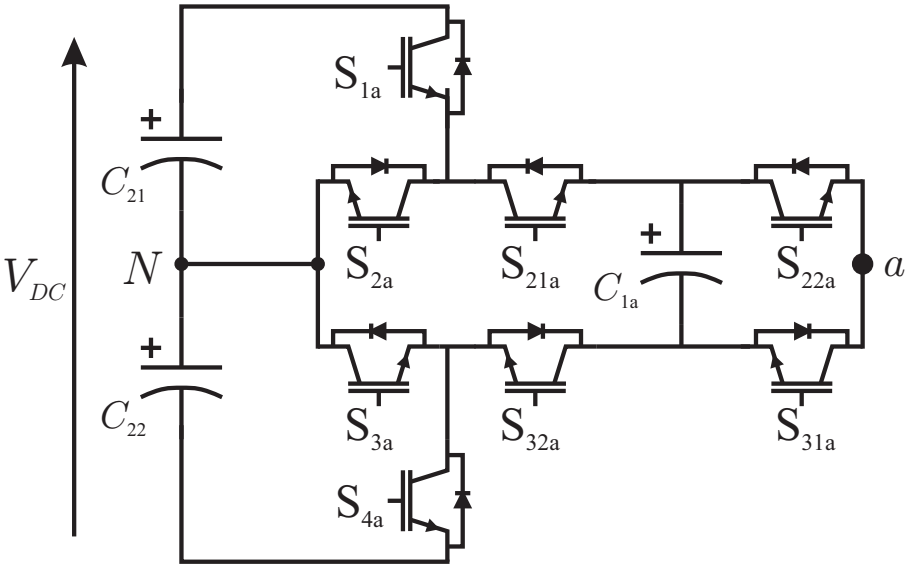


Figure 2.8. *1-Phase 5-level ANPC Inverter.*

The configuration of the ANPC allows the generation of five voltage levels at the output terminal of phase a, with respect to the neutral point N, considering the switching combinations given in Table 2.2. This topology needs a direct control over the inner voltage in the flying capacitor to ensure the correct performance, keeping the inner capacitor voltage to $V_{DC}/4$.

The power switches in 5L-ANPC does not have the same blocking voltage. The power switches S_{22a}, S_{31a}, S_{21a} and S_{32a} block $V_{DC}/4$, and the switches S_{1a}, S_{2a}, S_{3a}, and S_{4a} block $V_{DC}/2$.

2.2.2. Vectors generated by the inverter

Fig. 2.9 shows the possible switching states for phase a of ANPC, where power switches in grey color mean OFF state and power switches in black color mean ON state.

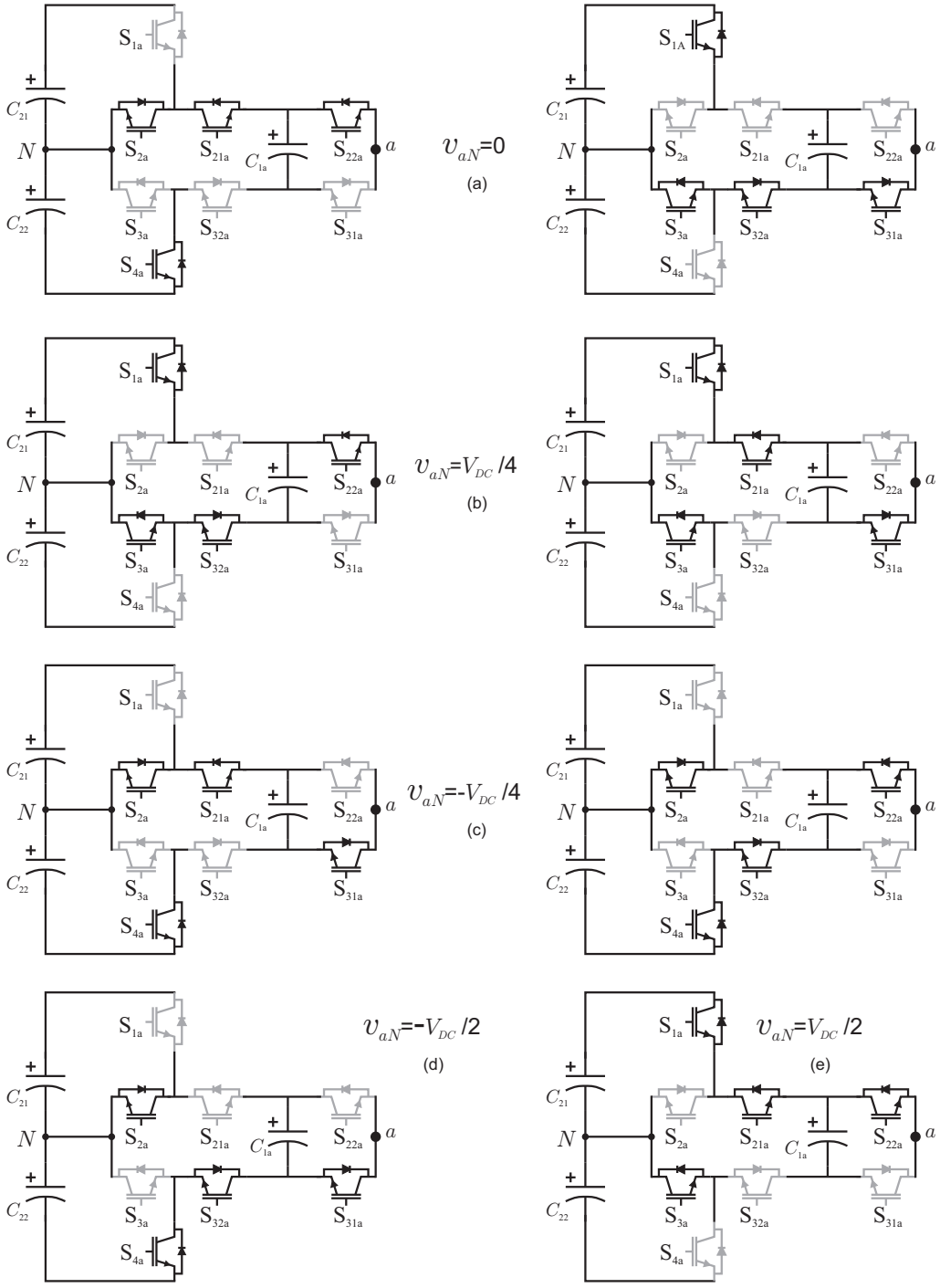


Figure 2.9. *Possible switching states of an 5L-ANPC: (a) Output voltage: 0; (b) Output voltage: $V_{DC}/4$; (c) Output voltage: $-V_{DC}/4$; (d) Output voltage: $-V_{DC}/2$; (e) Output voltage: $V_{DC}/2$.*

Table 2.2
Switching states for one phase of the ANPC inverter.

Voltage	Switches states								Output voltage
	S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{21a}	S_{32a}	S_{22a}	S_{31a}	
V_1	0	1	0	1	0	1	0	1	$-V_{DC}/2$
V_2	0	1	0	1	1	0	0	1	$-V_{DC}/4$
V_3	0	1	0	1	0	1	1	0	$-V_{DC}/4$
V_4	0	1	0	1	1	0	1	0	0
V_5	1	0	1	0	0	1	0	1	0
V_6	1	0	1	0	0	1	1	0	$V_{DC}/4$
V_7	1	0	1	0	1	0	0	1	$V_{DC}/4$
V_8	1	0	1	0	1	0	1	0	$V_{DC}/2$

Fig. 2.9-(a) show the circuit for voltages V_4 and V_5 indicated in Table 2.2, Fig. 2.9-(b) show the circuit for voltages V_6 and V_7, Fig. 2.9-(c) show the circuit for voltages V_2 and V_3, Fig. 2.9-(d) shows the circuit for vector V_1 and finally, Fig. 2.9-(e) shows the circuit for vector V_8 indicated in Table 2.2.

It is possible see that vectors V_2, V_3, V_6 and V_7, have influences on the inner voltage, charging or discharging the inner capacitor in function of the output current.

For the three phase inverter, $8^3 = 512$ switching states are generated. The 512 switching states produce 125 different voltage vectors, as shown in Fig. 2.10.

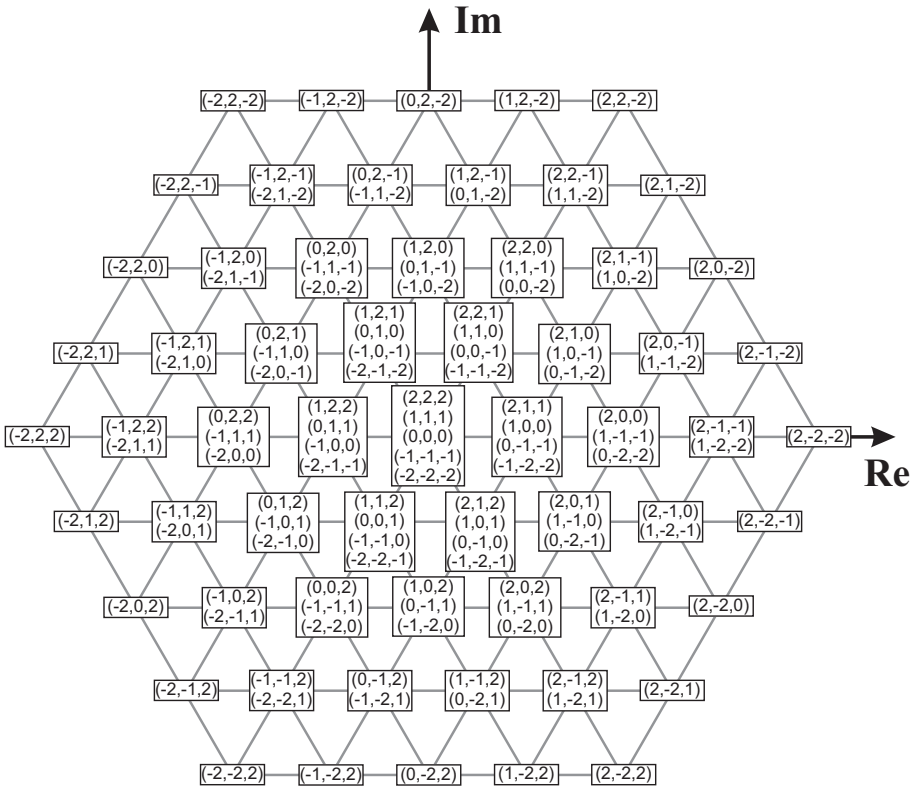


Figure 2.10. *Space vectors of 5L-ANPC.*

Some voltage vectors are redundant, generating the same voltage vector. For example, vector $\mathbf{V} = 0$ can be generated by five different voltage states (S): (2,2,2), (1,1,1), (0,0,0), (-1,-1,-1), and (-2,-2,-2). Where:

$$S = (S_a, S_b, S_c) \tag{2.9}$$

$$S_{a,b,c} \in \{2, 1, 0, -1, -2\} \tag{2.10}$$

$$\text{State } 2 \rightarrow v_{aN} = V_{DC}/2$$
$$\text{State } 1 \rightarrow v_{aN} = V_{DC}/4$$
$$\text{State } 0 \rightarrow v_{aN} = 0$$
$$\text{State -1} \rightarrow v_{aN} = -V_{DC}/4$$
$$\text{State -2} \rightarrow v_{aN} = -V_{DC}/2$$

2.2.3. The classical modulation

The classic modulation used in the 5L-ANPC is a Phase Shifted-PWM (PS-PWM) with $\phi = 180°$.

From Table 2.2, it can be seen that pair of power switches (S_{22a},S_{31a}), (S_{21a},S_{32a}), (S_{1a},S_{2a}), and (S_{3a},S_{4a}) are complementary switch pair and S_{1a} and S_{3a} require the same switching signal.

It can be seen that S_{1a} and S_{3a} are turned OFF when the output voltage is negative and turned ON when the output voltage is positive. So, the switch pairs (S_{1a},S_{2a}), and (S_{3a},S_{4a}) can be operated at fundamental frequency based on the polarity of the phase voltage.

For the switch pairs (S_{22a},S_{31a}) and (S_{21a},S_{32a}) a classic PS-PWM can be used to control them.

Fig 2.11 shows the block diagram for connecting the signals to the power switches using the PWM modulation, while Fig. 2.12 shows the waveforms for the classic modulation for a 5L-ANPC.

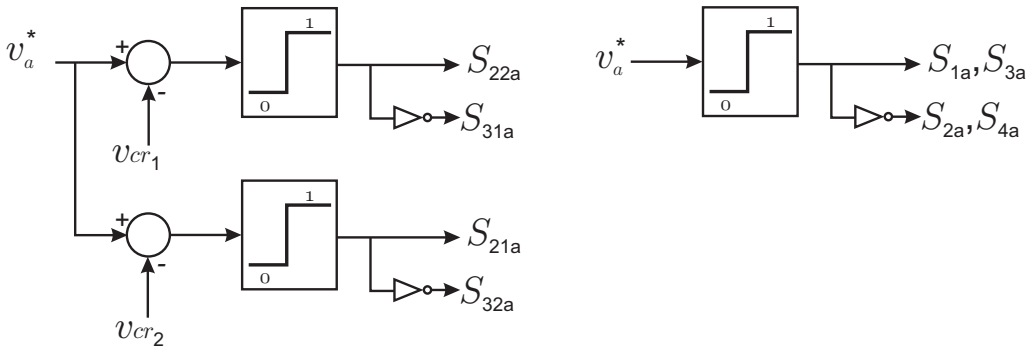


Figure 2.11. *Block diagram of PS-PWM modulation for a 5L-ANPC.*

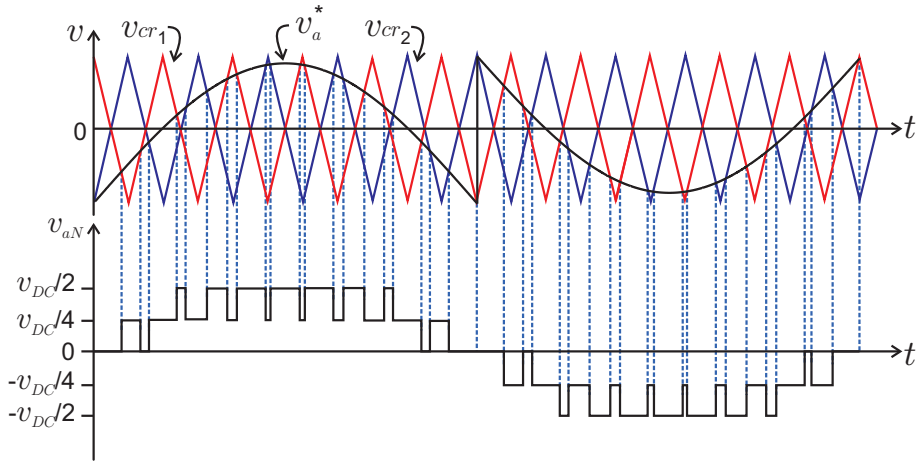


Figure 2.12. *Classic PWM modulation for a 5L-ANPC.*

2.2.4. Summary

The main advantages and disadvantages of this topology can be summarized as follows.

Advantages :

- It is more suitable for high-performance medium voltage motor drives [29–37].
- It can overcome the limitations of the NPC inverter by reducing the total numbers of capacitors necessary to generate 5-levels, which makes it easy to balance all voltages.
- It only needs one source of DC voltage to power all inverter. The midpoints can be obtained using capacitors.

Disadvantages :

- Depending on how the voltage *dc-link* V_{DC} is obtained, imbalances may arise between the capacitors. This drawback can be mitigated by modifying the control output switches.
- Since it has a larger number of semiconductor devices, it has higher conduction losses.
- To go to medium voltage applications it is necessary to duplicate power switches S_{1A}, S_{2A}, S_{3A} and S_{4A} in all phases to get same blocking voltage in all semiconductors.

2.3. Flying Capacitor Converter (FCC)

The FCC topology was developed in the 1990s [8] and it uses several floating capacitors instead of clamping diodes to share the voltage stress among devices and to achieve different voltage levels in the output.

The FCC topology can be extended achieving more levels in the output phase by the connection of more cells in tandem (see Fig. 2.13). Nowadays, the FCC has a reduced industrial presence, but some commercial products can be found as the converter ALSPA VDM6000 by Alstom [38, 39].

2.3.1. The power circuit

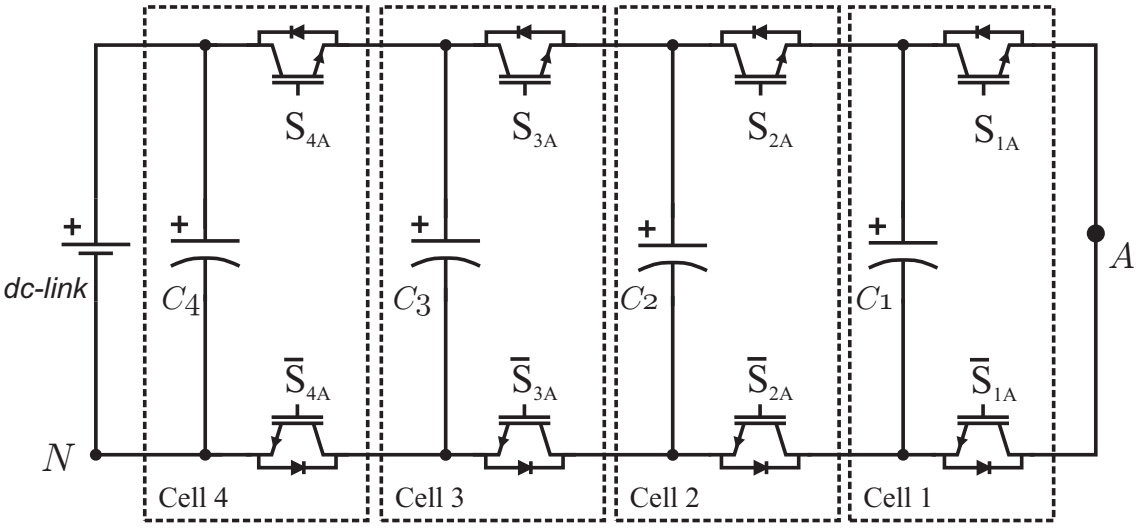


Figure 2.13. *1-Phase Inverter 5-level FCC.*

Fig. 2.13 shows the topology for a 5-level single-phase FCC, which is composed by the tandem connection of four basic units called *cells*.

Each cell requires a capacitor and two power switches, which must be operated complementary. In most works, the capacitor voltages ratio is set as $v_{C1} : v_{C2} : v_{C3} : v_{C4} = 1 : 2 : 3 : 4$. When this condition is reached, the converter generates a 5-level voltage waveform between the output terminal A and the inverter neutral point N. Other voltage ratios have been proposed in literature [40–42]; however, the standard $1 : 2 : 3 : 4$ ratio presents the advantage of obtaining an evenly spread voltage stress among the power switches.

Additionally, this standard ratio can be naturally achieved with a simple Phase Shifted Pulse Wide Modulation (PS-PWM) strategy, i.e., in an open-loop manner [43, 44].

2.3.2. Vectors generated by the inverter

Every cell of FCC can generate 2 possible states. In the case of a 5-level FCC with 4-cells, the total possible states are: $2^4 = 16$. Table 2.3 shows the possible states of the multilevel converter and the influence of the inner voltage on the output value.

Table 2.3
Switching states for one phase of the FCC.

Voltage	Switches states				Output voltage	Output voltage [V]
	S_{4a}	S_{3a}	S_{2a}	S_{1a}		
V_1	0	0	0	0	0	0
V_2	0	0	0	1	v_{C1}	
V_3	0	0	1	0	$v_{C2} - v_{C1}$	$V_{DC}/4$
V_4	0	1	0	0	$v_{C3} - v_{C2}$	
V_5	1	0	0	0	$v_{C4} - v_{C3}$	
V_6	0	0	1	1	v_{C2}	
V_7	0	1	1	0	$v_{C3} - v_{C1}$	
V_8	1	1	0	0	$v_{C4} - v_{C2}$	$V_{DC}/2$
V_9	0	1	0	1	$v_{C3} - v_{C2} + v_{C1}$	
V_{10}	1	0	0	1	$v_{C4} - v_{C3} + v_{C1}$	
V_{11}	1	0	1	0	$v_{C4} - v_{C3} + v_{C2} - v_{C1}$	
V_{12}	0	1	1	1	v_{C3}	
V_{13}	1	1	1	0	$v_{C4} - v_{C1}$	$3V_{DC}/4$
V_{14}	1	1	0	1	$v_{C4} - v_{C2} + v_{C1}$	
V_{15}	1	0	1	1	$v_{C4} - v_{C3} + v_{C2}$	
V_{16}	1	1	1	1	v_{C4}	V_{DC}

The redundance in the voltage states V_2, V_3, V_4 and V_5 for output level $V_{DC}/4$ and the redundance in the voltage states V_6, V_7, V_8, V_9, V_{10} and V_{11} for output level $V_{DC}/4$ and finally, the redundance in the voltage states V_12, V_{13}, V_{14} and V_{15} for output level $3V_{DC}/4$ allow getting an appropriate combination of switching states that ensures the correct inner voltage and the desired output voltage, charging or discharging the inner capacitor when is necessary.

For the 3-phase 5-level FCC there are $16^3 = 4096$ possible switching states. These switching states produce 125 different voltage vectors, as shown in Fig. 2.14.

Some voltage vectors are redundant, the vector $\mathbf{V} = 0$ can be generated by five different voltage states (S): (4,4,4), (3,3,3), (2,2,2), (1,1,1), and (0,0,0). Considering:

$$S = (S_a, S_b, S_c) \tag{2.11}$$

$$S_{a,b,c} \in \{4, 3, 2, 1, 0\} \tag{2.12}$$

$$\text{State } 4 \rightarrow v_{aN} = V_{DC}$$
$$\text{State } 3 \rightarrow v_{aN} = 3V_{DC}/4$$
$$\text{State } 2 \rightarrow v_{aN} = V_{DC}/2$$
$$\text{State } 1 \rightarrow v_{aN} = V_{DC}/4$$
$$\text{State } 0 \rightarrow v_{aN} = 0$$

2.3.3. The classical modulation

The classic PWM modulation of the FCC that allows to balance the inner voltage is a special technique called: *Phase Shifted PWM* (PS-PWM). The phase shifted between the

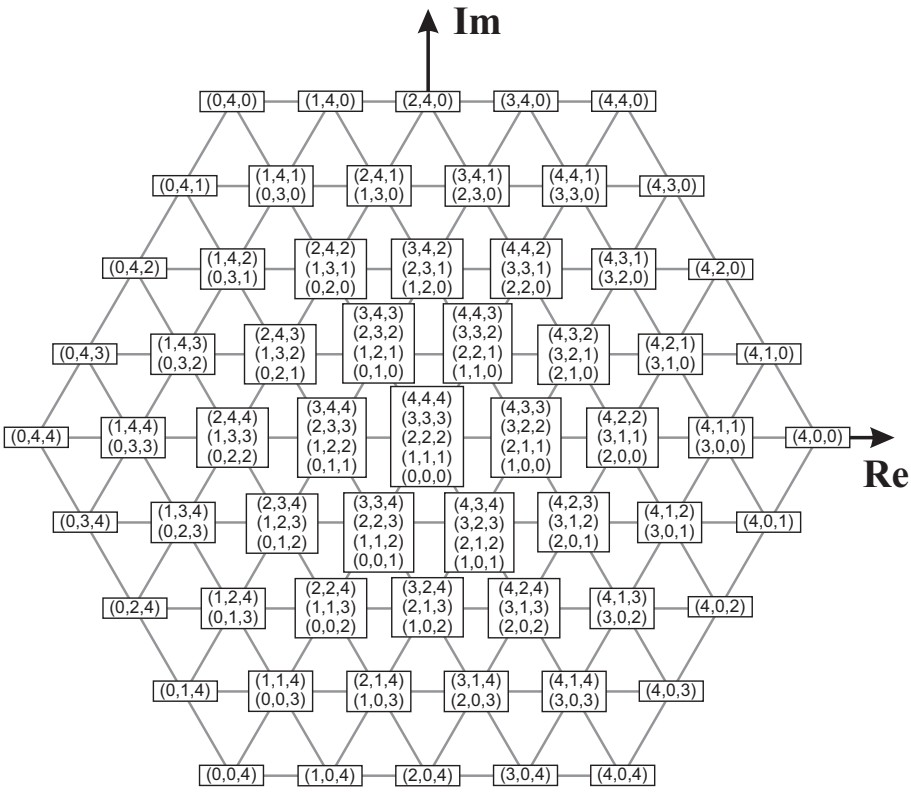


Figure 2.14. *Space vectors of 5L-FFC.*

carrier signal in a FCC is given by the expression:

$$\phi = \frac{360}{N_c} \tag{2.13}$$

Where N_c is the number of cells in the topology. In the case of 5-level FCC, $\phi = 90°$.

Fig 2.15 shows the block diagram to generate the signals to the power switches employing a PS-PWM modulation, where v_a^* is the reference signal for the output phase a and v_{cr_i} for all $i \in \{1, 2, 3, 4\}$ are the carrier signals. Fig. 2.16 shows the classic PS-PWM waveform.

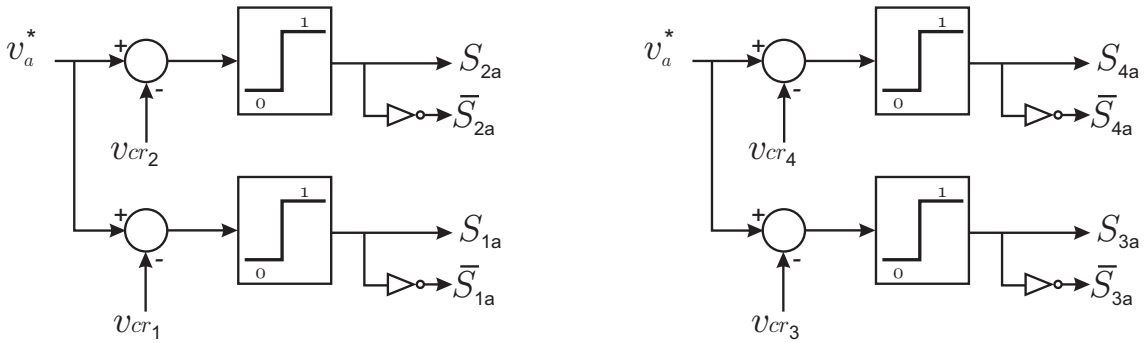


Figure 2.15. *Block diagram of PS-PWM modulation for a 5-level FCC.*

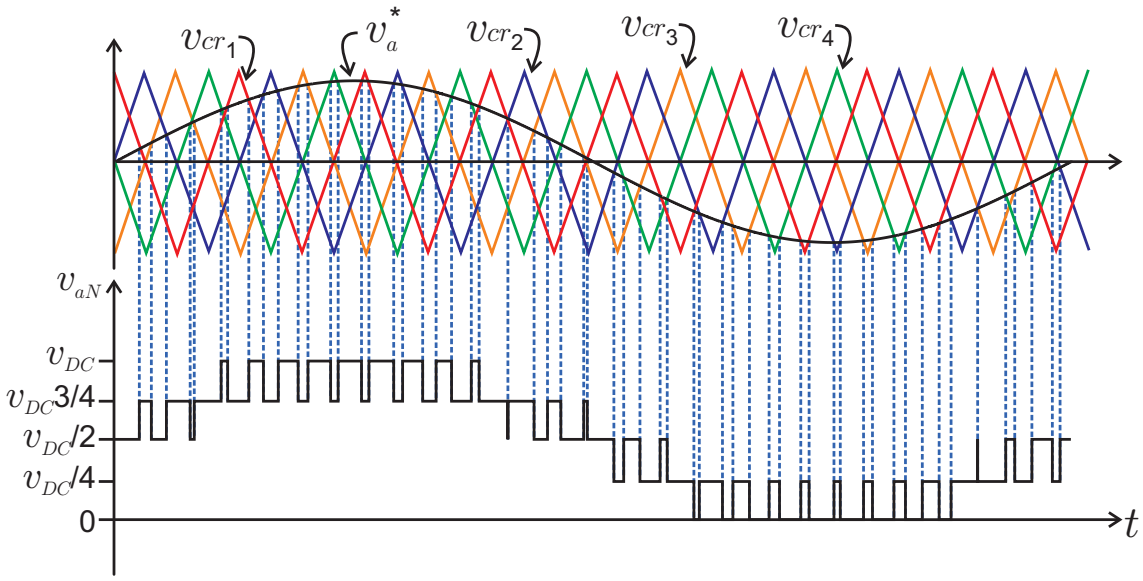


Figure 2.16. *Classic Phase Shifted-PWM modulation.*

2.3.4. Summary

The main advantages and disadvantages of this topology can be summarized as follows.

Advantages :

- The large number of capacitors provides a source of energy storage, which increases the availability of the system against momentary loss of power of the grid.
- In case of failure, removing cells does not decrease the maximum voltage applied, the only consequence is the reduction of levels obtained at the output and the increase of blocking voltage in the semiconductors and the voltage in the capacitors.
- FCC has a modular configuration, which makes it a *scalable* converter.

Disadvantages :

- The number, size and voltage rating of capacitors increases with the number of levels, these being one of the components that make up the FCC of lesser life and higher cost, in addition to increasing the size of the inverter.
- The main capacitor must be designed to withstand the maximum voltage. In the case of a very high voltage, it is necessary to resort to configurations of the arrangement of capacitors.
- Large commutation loops whose stray inductances cause high voltages overshoots.
- Like the NPC configuration, in this inverter special considerations must be taken in the implementation of the control to ensure a correct balance of the voltages of the flying capacitors. [45, 46]

2.4. Stacked Multicell Converter (SMC)

Today, the 3-phase 5-level SMC topology has a commercial application in medium voltage with the MV6 series from GE Power Conversion.

2.4.1. The power circuit

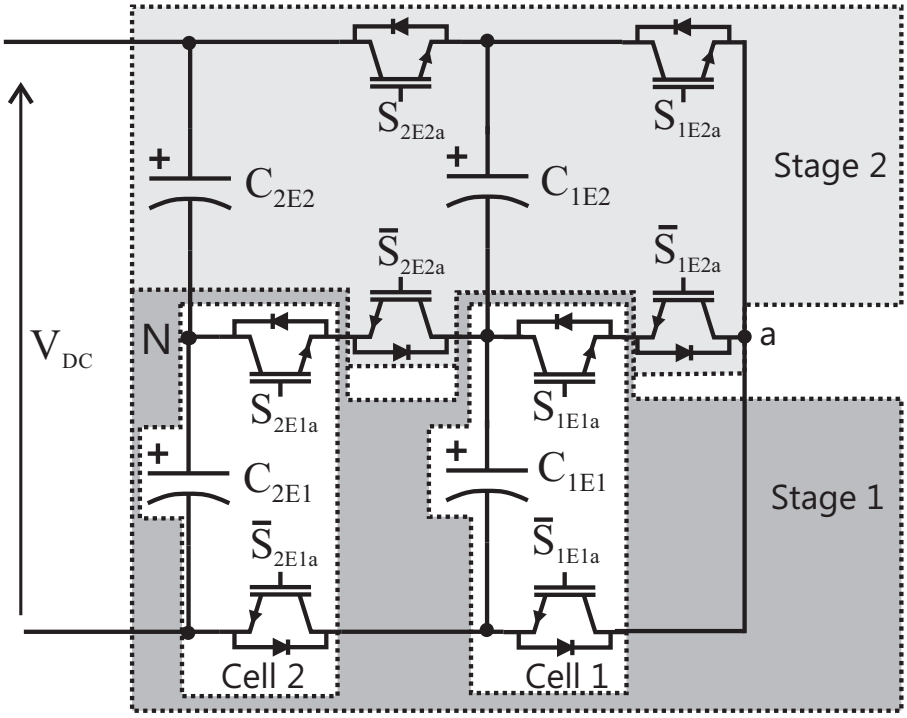


Figure 2.17. *Topology of one phase of a Stacked Multicell Converter 2x2.*

Fig. 2.17 presents the power circuit of the 5L-SMC converter for one phase, which is based on a hybrid association of elementary commutation cells. Each of these cells requires a capacitor and two power switches, which must be operated complementary.

Each stage (n cells stacked vertically) of the full converter can be viewed as a classical multicell converter (Flying Capacitor Converter) having p commutation cells in series.

Fig. 2.17 is the particular case when $p = 2$ cells (horizontal) and $n = 2$ stages (vertical). For this converter four flying capacitors C_{iEj} with $i \in \{1, 2\}$ and $j \in \{1, 2\}$ appear, where i indicates the number of the respective cell (cells put horizontally) while j indicates the number of the respective stage (cells put vertically). Each voltage across these capacitors is then equal to $V_{C_{iEj}} = \frac{i \cdot E}{n \cdot p}$ with $E = V_{DC}$ the input voltage of the converter.

2.4.2. Vectors generated by the inverter

The SMC 2x2 shown in Fig. 2.17 has $N_{states} = 9$ different states and $N_{levels} = 5$ different levels in the output. These 9 configurations and their respective levels considering the particular case of the SMC 2x2, $V_{C_{2E2a}} = V_{C_{2E1a}}$; $V_{C_{1E2a}} = V_{C_{1E1a}}$; $E = V_{DC}$ and

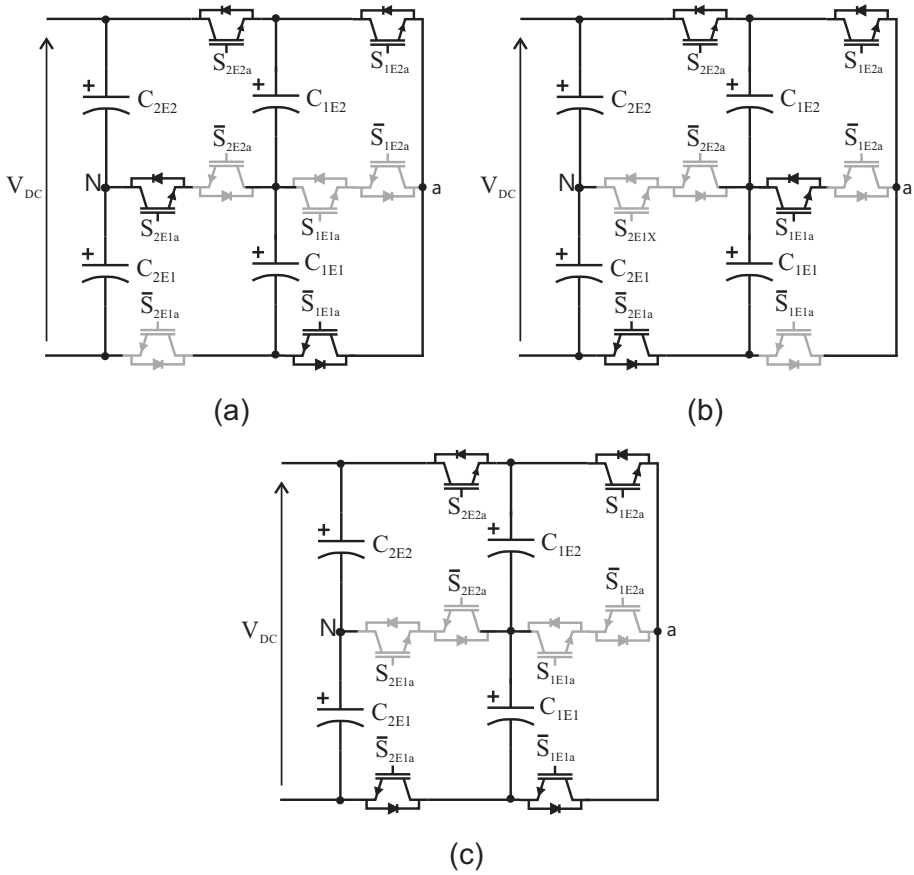


Figure 2.18. *Switching states not allowed in a SMC 2x2: (a) Short circuit in cell 1; (b) Short circuit in cell 2; (c) Short circuit in both cells.*

$V_{DC} : V_{C_{2E1a}} : V_{C_{1E1a}} = 4 : 2 : 1$, are shown in Table 2.4, where $S_{iEja} = 1$ when switch S_{iEja} is ON, and $S_{iEja} = 0$ when switch S_{iEja} is OFF.

Table 2.4
Switching states for one phase of the Stacked Multicell Converter 2x2

Voltage	**State** $(S_{2E2a}, S_{2E1a}, S_{1E2a}, S_{1E1a})$	**Output Voltage** v_{aN}	**Output Voltage** v_{aN} [V]
V_1	(0,0,0,0)	$-V_{C_{2E1a}}$	$-V_{DC}/2$
V_2	(0,0,0,1)	$V_{C_{1E1a}} - V_{C_{2E1a}}$	$-V_{DC}/4$
V_3	(0,0,1,1)	$V_{C_{1E2a}} + V_{C_{1E1a}} - V_{C_{2E1a}}$	0
V_4	(0,1,0,0)	$-V_{C_{1E1a}}$	$-V_{DC}/4$
V_5	(0,1,0,1)	0	0
V_6	(0,1,1,1)	$V_{C_{1E2a}}$	$V_{DC}/4$
V_7	(1,1,0,0)	$V_{C_{2E2a}} - V_{C_{1E2a}} - V_{C_{1E1a}}$	0
V_8	(1,1,0,1)	$V_{C_{2E2a}} - V_{C_{1E2a}}$	$V_{DC}/4$
V_9	(1,1,1,1)	$V_{C_{2E2a}}$	$V_{DC}/2$

Each power switch can take only two possible states, so, if SMC has four switches (not considering the complementary pair) then it will have $N_{states} = 4^2 = 16$ possible states. But this argument is not valid, because there are 7 switching states not allowed. The state when the switch of the upper stage is ON ($S_{jE2a} = 1$) and the switch of the lower stage is OFF ($S_{jE1a} = 0$) (see Fig. 2.18) generates a short circuit through both capacitors of the stage j. Consequently, the total states for each cell of both stages (ex. cell 1 of the stage 1 and cell 1 of the stage 2) is 3 instead of $N_{states_{cell1}} = 2^2 = 4$, so the total states of the an SMC 2x2 will be $N_{states} = 3^2 = 9$ because it has three states for each cells and has two cells.

Generalizing, the number of possible states of the circuit is then equal to:

$$N_{states} = (n+1)^p \tag{2.14}$$

The number of levels in a SMC for the output voltage is equal to:

$$N_{levels} = (np) + 1 \tag{2.15}$$

The 3-phase 5L-FCC has $9^3 = 729$ switching states and these 729 switching states produce 125 different voltage vectors, the same as like in 5L-ANPC, as shown in Fig. 2.10.

2.4.3. The classical modulation

It is necessary to define the global referential signal called v_rg. This signal corresponds to the reference for the output voltage of the converter.

Based on this signal v_rg and on the number of stages ($n = 2$), n signals of internal references (called v_{rEj}) can be generated. These signals v_{rEj} will be send to each stage ($n = 2$) of the converter, then each signals v_{rEj} are modulated with PS-PWM strategy for each stage.

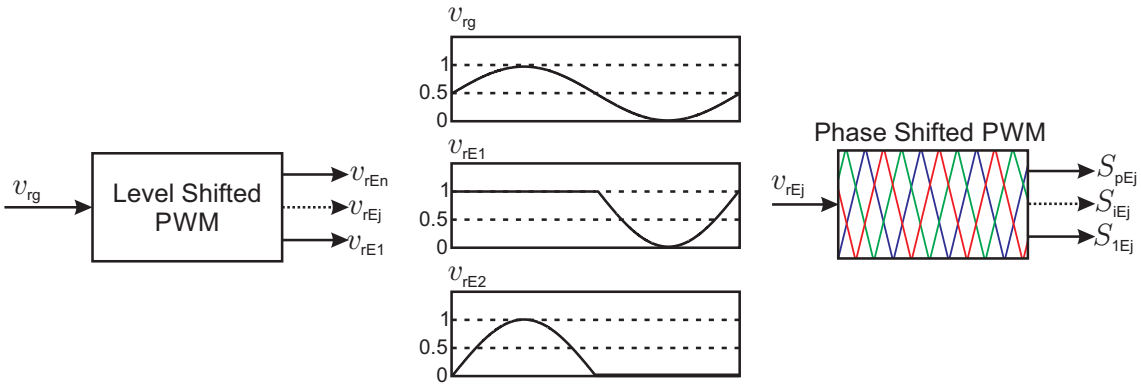


Figure 2.19. *Steps in the classical modulation of the SMC.*

Consequently, the classical modulation of the SMC requires two steps. The first step modulates v_rg signal for each stages of the SMC (in vertical) to determinate the internal reference signals (called v_{rEj}), the second step modulates v_{rEj} signals for each cell of each stages (in horizontal). Being the resulting modulation a Mixed Shifted-PWM, which is composed of a Phase Shifted-PWM (PS-PWM) determined for the numbers of cells that

compose each stage (two cells horizontal in the case of the SMC 2x2), and a Level Shifted-PWM (LP-PWM) determined by the numbers of stages that compose the converter (two stages vertical in the case of the SMC 2x2).

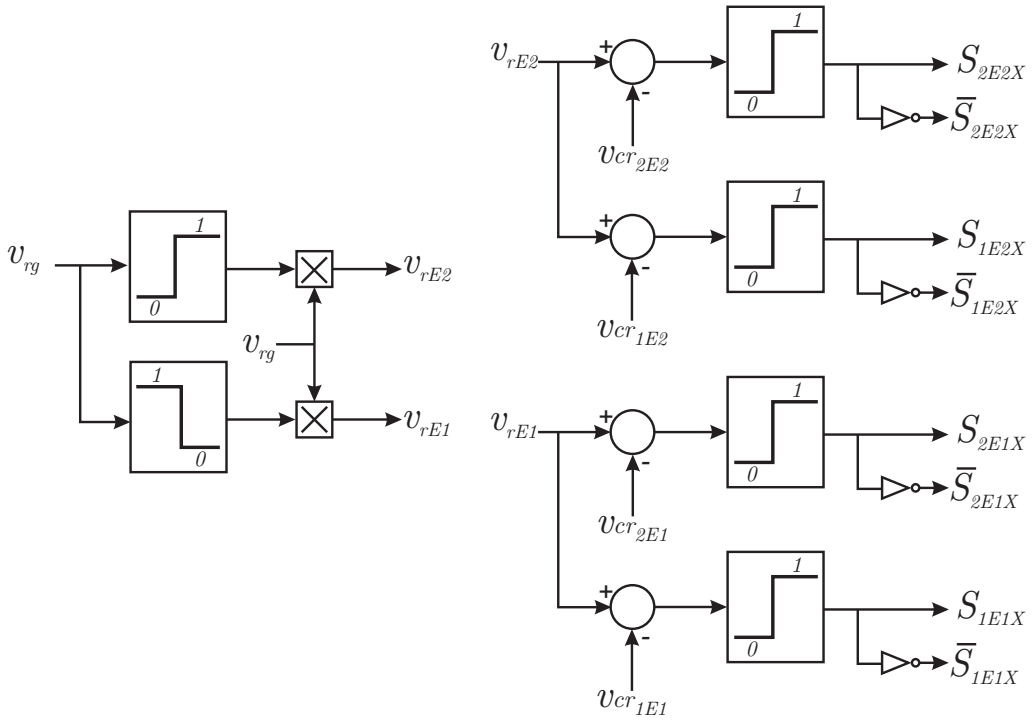


Figure 2.20. *Block diagram of the classical modulation for a SMC 2x2.*

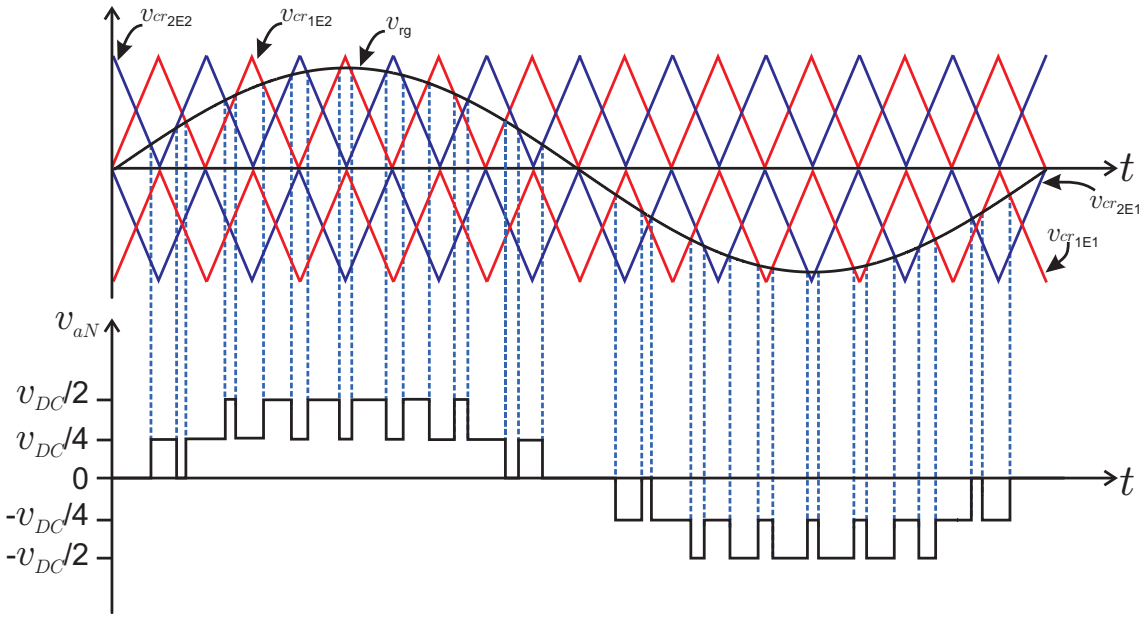


Figure 2.21. *Classical modulation of a SMC 2x2.*

Fig. 2.19 shows the steps for the classical modulation of a SMC with n stages and p cells, where the first step to determinate the voltage reference for the each vertical stages

(v_{rEj}) is a LS-PWM.

Fig. 2.20 shows the block diagram of the classical modulation for a SMC with 2 stacks and 2 cells. Fig. 2.21 shows the classical modulation in the particular case of a SMC 2x2.

2.4.4. Summary

The main advantages and disadvantages of this topology can be summarized as follows.

Advantages :

- Capacitors are smaller than those used in FCC. In 5L-SMC it is necessary two capacitor blocking $V_{DC}/4$ and two blocking $V_{DC}/2$ and in 5L-FCC it is necessary one capacitor blocking $V_{DC}/4$, one blocking $V_{DC}/2$, one blocking $3V_{DC}/4$ and finally one for the *dc-link* (V_{DC}).
- Large number of levels to the output of converter with good dynamic of current and power.
- The number of degrees of freedom increases as well as the levels per cell.
- Converter with modular configuration feature that makes it a scalable converter.

Disadvantages :

- More power semiconductor per cell than in a classical multicell converter.
- A lot of flying capacitors that need to be balanced.

Chapter 3

Reduced Multilevel Converter

The Reduced Multilevel Converter (RMC) [47] structure concept is composed by a variable *dc-link* converter and 3-phase output inverter stage, like the one shown in Fig. 3.1 for a 5 level configuration using a 2L-VSI. The variable *dc-link* structure is composed by a cascaded connection of basic units called *DC-cell* which is shown in Fig. 3.2.

Every DC-cell is formed by three power switches and one capacitor, when the power switch in series with the capacitor (S_{Ck}) is ON, the upper and lower switches (S_{pk} and S_{nk}) must to work in a complementary way to avoid short circuit.

One way to understand how this topology works is to imagine it as two parts that work together. One (the DC-cells) works as a DC-DC multilevel converter, generating a variable *dc-link* between the points p and n, and the second part (output inverter) works as a DC-AC inverter connected to a variable *dc-link* and can be any inverter with a single DC-bus configuration like the 2L-VSI, NPC, 3L-ANPC, 5L-ANPC, T-type (SMC 1x2) [13], FCC, SMC.

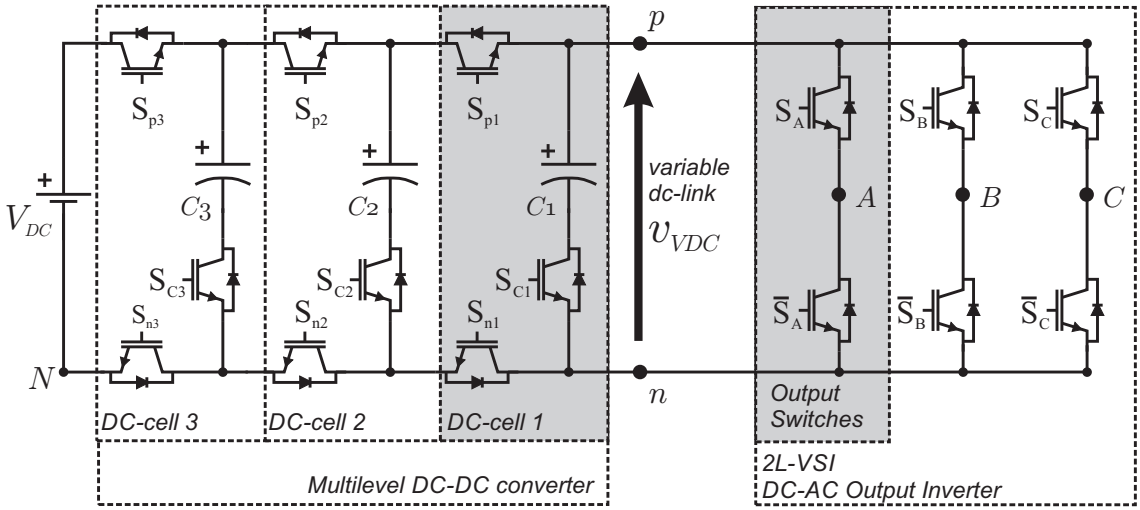


Figure 3.1. *Five Level Reduced Multilevel Converter (5L-RMC), with 3 DC-cell and a 2L-VSI output inverter.*

In this work, the basic 2L-VSI is used for simplicity. The 2L-VSI is connected to the

variable *dc-link* and can chooses the output voltage between two options: v_{pN} or v_{nN} as shown in Fig. 3.1.

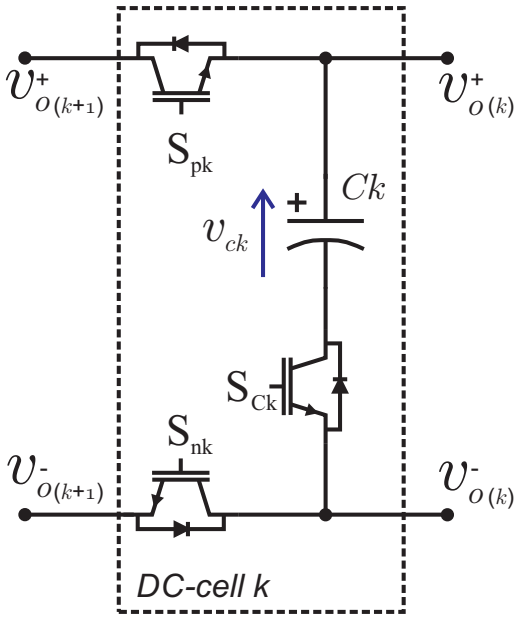


Figure 3.2. *Generic DC-cell k of RMC.*

3.1. Basic properties

The RMC is a modular multicell structure, much like the FCC and SMC; this means that it is possible to increase (reduce) the number of levels by connecting (disconnecting) DC-cell units following the multicell arrangement.

Every main cell, see Fig. 3.2, has three possible conduction states as shown in Table 3.1, where $S_{pk} = 1$ means that the power switch pk is ON and $S_{pk} = 0$ means that it is OFF, for all power switches S_{pk}, S_{nk} and S_{Ck}.

Table 3.1
DC-cell RMC: Possible switching states

Switching State			**Output Potential**	
S_{pk}	S_{nk}	S_{Ck}	$v^{+}_{o(k)}$	$v^{-}_{o(k)}$
1	1	0	$v^{+}_{o(k+1)}$	$v^{-}_{o(k+1)}$
0	1	1	$v^{-}_{o(k+1)} + v_{ck}$	$v^{-}_{o(k+1)}$
1	0	1	$v^{+}_{o(k+1)}$	$v^{+}_{o(k+1)} - v_{ck}$

Hence, each additional DC-cell incorporates three possible switching states for the DC-DC multilevel part of the converter and the total possible states can be expressed as an equation in function of the number of DC-cells ($N_{DC-cell}$) as follows:

$$N_{states_{DC-DC}} = 3^{N_{DC-cell}} \tag{3.1}$$

In the case of the RMC shown in Fig. 3.1, there are 3 DC-cells and the possible switching states for the DC-DC multilevel part are $3^3 = 27$.

For the DC-AC inverter part is used a 2L-VSI and there are two power switches for each output phase. These two switches work in a complementary way, when $S_x = 1$, i.e. it is ON, the switch $\bar{S}_x = 0$, is OFF. This is necessary, because $S_x = 1$ and $\bar{S}_x = 1$ at the same time generate a short circuit in the variable dc-link, that is in the dc-link or in one of the inner capacitors.

The possible switching states for each phase is 2. Therefore, the number of possible states in function of the number of output phases (N_{OP}) can be described by:

$$N_{states_{DC-AC}} = 2^{N_{OP}} \tag{3.2}$$

In the case of the RMC shown in Fig. 3.1, there are 3 output phases and the possible switching states for the DC-AC part is $2^3 = 8$.

The total number of possible states of the whole converter is given by the multiplication of the number of states in the DC-DC multilevel part and in the DC-AC part as in equation (3.3):

$$N_{states} = N_{states_{DC-DC}} * N_{states_{DC-AC}} \tag{3.3}$$

For the case of a 5-level, 3-phase RMC shown in Fig. 3.1, the total possible states are $N_{states} = 27 * 8 = 216$.

The number of output voltages (N_{OV}) between the output phase (A, B or C) and the neutral point of the converter (N) is given by:

$$N_{OV} = N_{DC-cell} + 2 \tag{3.4}$$

As long as the inner voltage in the capacitors follows the relationship given by:

$$v_{Ck} = k\frac{V_{DC}}{N_{DC-cell} + 1} \tag{3.5}$$

All possible combination of these 216 possible switching states generates 65 output voltage vectors, which are shown in Fig. 3.3. Where the voltage vectors are described by the variable S as follow:

$$S = (S_A, S_B, S_C) \tag{3.6}$$

$$S_{a,b,c} \in \{4, 3, 2, 1, 0\} \tag{3.7}$$

$$\text{State } 4 \rightarrow v_{aN} = V_{DC}$$
$$\text{State } 3 \rightarrow v_{aN} = 3V_{DC}/4$$
$$\text{State } 2 \rightarrow v_{aN} = V_{DC}/2$$
$$\text{State } 1 \rightarrow v_{aN} = V_{DC}/4$$
$$\text{State } 0 \rightarrow v_{aN} = 0$$

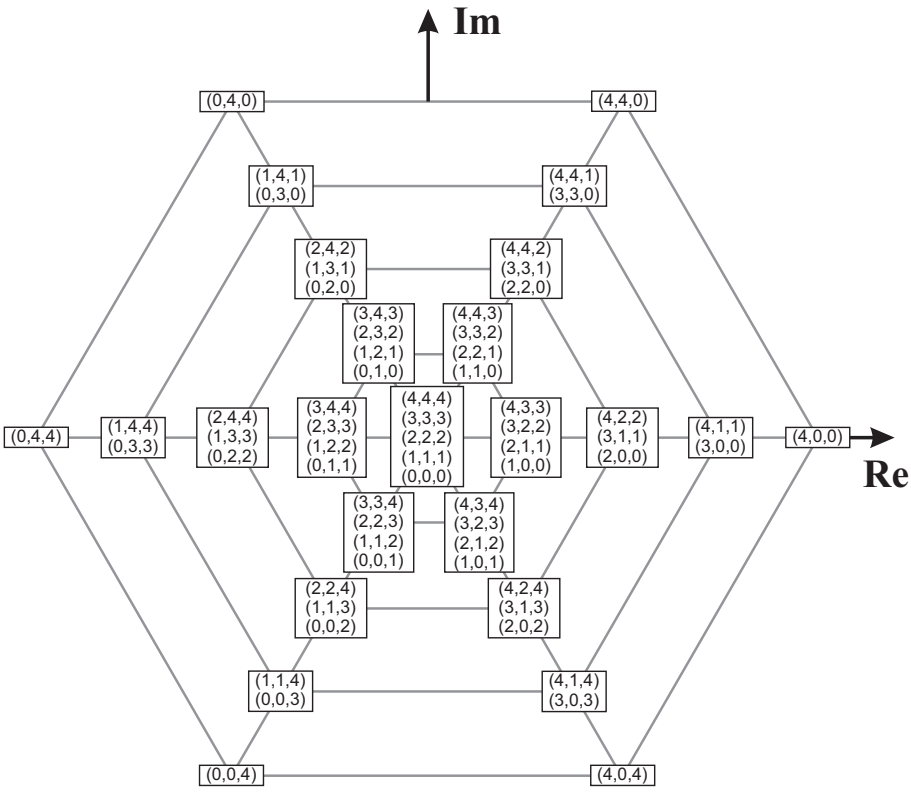


Figure 3.3. *Total possible output voltage vector in 5L-RMC.*

There are 54 possible switching states for the voltage vector zero, 18 possible switching states for all possible voltage vector in the first ring, 6 possible switching states for all voltage vector in the second ring, 2 for the third ring and only one possible switching state for the vectors in the final ring as is summary in Table 3.2.

Table 3.2
Redundant Switching States for all possible output voltage levels

Number of possible Switching States	Output voltage magnitude
54	0 [V]
$18 \cdot 6 = 108$	$V_{DC}/6$ [V]
$6 \cdot 6 = 36$	$V_{DC}/3$ [V]
$2 \cdot 6 = 12$	$V_{DC}/2$ [V]
$1 \cdot 6 = 6$	$2V_{DC}/3$ [V]

Table 3.3 presents the 27 possible switching state of 3DC-cell RMC with the 54 possible output voltage for one phase (choosing $S_x = 1$ or $S_x = 0$ for the 2L-VSI).

Switching states in voltage $V_2 - V_5$ in Table 3.3 are redundant and generate the output voltage $v_{pN} = V_{DC}$ and $v_{nN} = 3V_{DC}/4$. Voltage $V_6 - V_7$ are redundant switching states and generate the output voltage $v_{pN} = V_{DC}$ and $v_{nN} = V_{DC}/2$. Switching states in voltage V_8 generates the output voltage $v_{pN} = V_{DC}$ and $v_{nN} = V_{DC}/4$. Switching states in voltage $V_9 - V_{13}$ generate the output voltage $v_{pN} = 3V_{DC}/4$ and $v_{nN} = V_{DC}/2$ with voltages

Table 3.3
Switching states for 3-MCs 5-level Reduced Multilevel Converter.

Voltage	Switches states						Output voltage	
	S_{p3}	S_{C3}	S_{p2}	S_{C2}	S_{p1}	S_{C1}	$S_x = 1$ (v_{pN})	$S_x = 0$ (v_{nN})
V_1	1	0	1	0	1	0	V_{DC}	0
V_2	1	0	1	0	1	1	V_{DC}	$V_{DC} - v_{C1}$
V_3	1	0	1	1	1	1	V_{DC}	$V_{DC} - v_{C1}$
V_4	1	1	1	0	1	1	V_{DC}	$V_{DC} - v_{C1}$
V_5	1	1	1	1	1	1	V_{DC}	$V_{DC} - v_{C1}$
V_6	1	1	1	1	1	0	V_{DC}	$V_{DC} - v_{C2}$
V_7	1	0	1	1	1	0	V_{DC}	$V_{DC} - v_{C2}$
V_8	1	1	1	0	1	0	V_{DC}	$V_{DC} - v_{C3}$
V_9	1	0	1	1	0	1	$V_{DC} - v_{C2} + v_{C1}$	$V_{DC} - v_{C2}$
V_{10}	1	1	1	1	0	1	$V_{DC} - v_{C2} + v_{C1}$	$V_{DC} - v_{C2}$
V_{11}	1	1	0	1	1	1	$V_{DC} - v_{C3} + v_{C2}$	$V_{DC} - v_{C3} + v_{C2} - v_{C1}$
V_{12}	0	1	1	0	1	1	v_{C3}	$v_{C3} - v_{C1}$
V_{13}	0	1	1	1	1	1	v_{C3}	$v_{C3} - v_{C1}$
V_{14}	1	1	0	1	1	0	$V_{DC} - v_{C3} + v_{C2}$	$V_{DC} - v_{C3}$
V_{15}	0	1	1	1	1	0	v_{C3}	$v_{C3} - v_{C2}$
V_{16}	0	1	1	0	1	0	v_{C3}	0
V_{17}	1	1	1	0	0	1	$V_{DC} - v_{C3} + v_{C1}$	$V_{DC} - v_{C3}$
V_{18}	1	1	0	1	0	1	$V_{DC} - v_{C3} + v_{C1}$	$V_{DC} - v_{C3}$
V_{19}	0	1	1	1	0	1	$v_{C3} - v_{C2} + v_{C1}$	$v_{C3} - v_{C2}$
V_{20}	1	0	0	1	1	1	v_{C2}	$v_{C2} - v_{C1}$
V_{21}	0	1	0	1	1	1	v_{C2}	$v_{C2} - v_{C1}$
V_{22}	1	0	0	1	1	0	v_{C2}	0
V_{23}	0	1	0	1	1	0	v_{C2}	0
V_{24}	1	0	1	0	0	1	v_{C1}	0
V_{25}	1	0	0	1	0	1	v_{C1}	0
V_{26}	0	1	1	0	0	1	v_{C1}	0
V_{27}	0	1	0	1	0	1	v_{C1}	0

$V_9 - V_{10}$ and voltages $V_{12} - V_{13}$ respectively redundant. Switching states in voltage $V_{14} - V_{15}$ generate the output voltage $v_{pN} = 3V_{DC}/4$ and $v_{nN} = V_{DC}/4$. Voltage V_{16} generates the output voltage $v_{pN} = 3V_{DC}/4$ and $v_{nN} = 0$. Switching states in voltage $V_{17} - V_{21}$ generate the output voltage $v_{pN} = V_{DC}/2$ and $v_{nN} = V_{DC}/4$ with voltages $V_{17} - V_{18}$ and voltages $V_{20} - V_{21}$ respectively redundant. Switching states in voltage $V_{22} - V_{23}$ are redundant switching states and generate the output voltage $v_{pN} = V_{DC}/2$ and $v_{nN} = 0$. And finally, switching states in voltage $V_{24} - V_{27}$ are redundant switching states and generate the output voltage $v_{pN} = V_{DC}/4$ and $v_{nN} = 0$.

This redundant switching states are summarized in Table 3.4.

Table 3.4
Redundant Switching States for 3DC-cell RMC

Switching States	Output voltage	
	v_{pN}	v_{nN}
$V_2 - V_5$	V_{DC}	$3V_{DC}/4$
$V_6 - V_7$	V_{DC}	$V_{DC}/2$
V_8	V_{DC}	$V_{DC}/4$
V_1	V_{DC}	0
$V_9 - V_{13}$	$3V_{DC}/4$	$V_{DC}/2$
$V_{14} - V_{15}$	$3V_{DC}/4$	$V_{DC}/4$
V_{16}	$3V_{DC}/4$	0
$V_{17} - V_{21}$	$V_{DC}/2$	$V_{DC}/4$
$V_{22} - V_{23}$	$V_{DC}/2$	0
$V_{24} - V_{27}$	$V_{DC}/4$	0

3.2. Operation principle

From the 27 allowed variable dc-link switching states, only 10 generate different voltage potentials in the output terminals (the 17 other generate redundant levels) for a three DC-cell RMC.

All combinations of these DC-DC multilevel voltages using a 2L-VSI in the dc-ac stage, gives a total of 216 possible output voltage space vectors, which are shown in Fig. 3.4 including the number of their redundancies.

Fig. 3.5 shows a selections of the 10 different dc-link level generation possibilities. Fig. 3.5-(a) to Fig. 3.5-(d) show the possible combinations for $v_{nN} = 0$ and $v_{pN} = V_{DC}/4$, $v_{pN} = V_{DC}/2$, $v_{pN} = 3V_{DC}/4$, and $v_{pN} = V_{DC}$ respectively. Fig. 3.5-(e) to Fig. 3.5-(g) show possible combinations for $v_{pN} = V_{DC}$ and: $v_{nN} = 3V_{DC}/4$, $v_{nN} = V_{DC}/2$, and $v_{nN} = V_{DC}/4$ respectively. Fig. 3.5-(h) and Fig. 3.5-(i) show possible combinations of $v_{pN} = 3V_{DC}/4$ and: $v_{nN} = V_{DC}/4$, and $v_{nN} = V_{DC}/2$ respectively. Finally, Fig. 3.5-(j) shows the combination of DC-DC voltage of $v_{pN} = V_{DC}/2$ and $v_{nN} = V_{DC}/4$.

To generate five voltage levels with the same voltage step (dv/dt), the voltages in the inner capacitors must follow the following ratio: $v_{C4} : v_{C3} : v_{C2} : v_{C1} = 4 : 3 : 2 : 1$, being $v_{C4} = V_{DC}$.

For simplicity and a better explanation, will be analysed the operation principle of 1DC-cell RMC, which is a 3-level topology. The possible DC-DC voltage combinations in a 3-level RMC is shown in Fig. 3.6. In this case, the inner voltage on capacitor C_1 is set to $V_{DC}/2$.

Fig. 3.6-(a) and Fig. 3.6-(b) generate the same voltage in the variable *dc-link* ($v_{VDC} = v_{C1} = V_{DC}/2$) however, the possible output voltages are different, for v_{pN} the output voltage is $V_{DC}/2$ or V_{DC}, respectively, and for v_{nN} the output voltage is 0 or $V_{DC}/2$, respectively. Finally, in Fig. 3.6-(c) the switching states generate a v_{VDC} equal to the main *dc-link*, i.e. $v_{VDC} = V_{DC}$ and the output voltages can be $v_{pN} = V_{DC}$ or $v_{nN} = 0$.

Using these combinations of switching states, it is possible to have whichever of the 3 possible output voltages 0, $V_{DC}/2$ or V_{DC}. This freedom allows, for example, to have two output phases with different modulation index (m_A and m_B), phase or frequency, as is shown in Fig. 3.7-(a), (b) and (c) respectively.

This operation characteristic ensures the same behavior as in standard multilevel converters as the FCC (see section 2.3), where one independent converter connected at the same *dc-link* for every phase is used. However, the reduction of necessary components in the proposed topology has a cost.In this case, a lower number of power switches means less possible switching states and therefore, less possible combinations that allow to balance the inner voltage. A consequence can be seen in Fig. 3.7, where sometimes it is necessary to make a double step in the output voltage (from $v_{AN} = 0$ to $v_{AN} = V_{DC}$) to achieve the desired inner voltage in the capacitor.

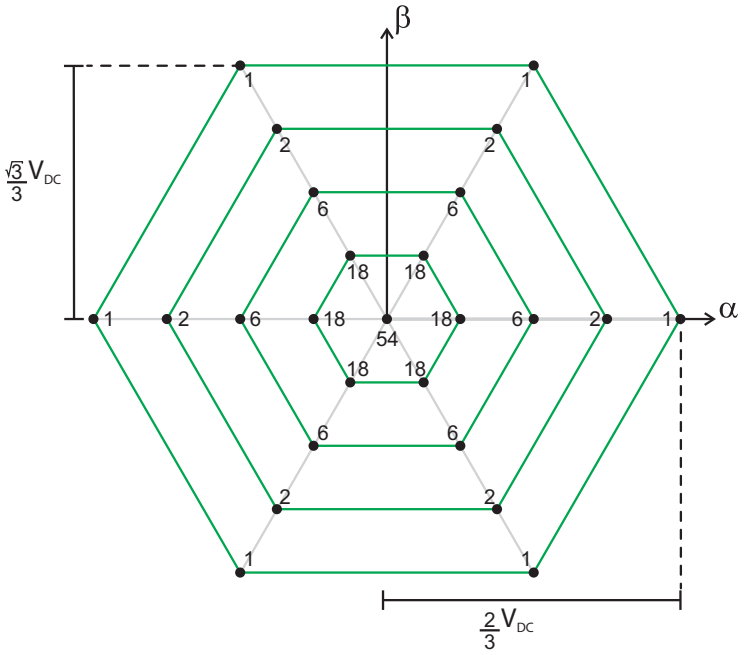


Figure 3.4. *Output voltage space vectors generated by the RMC, including their number of redundancies.*

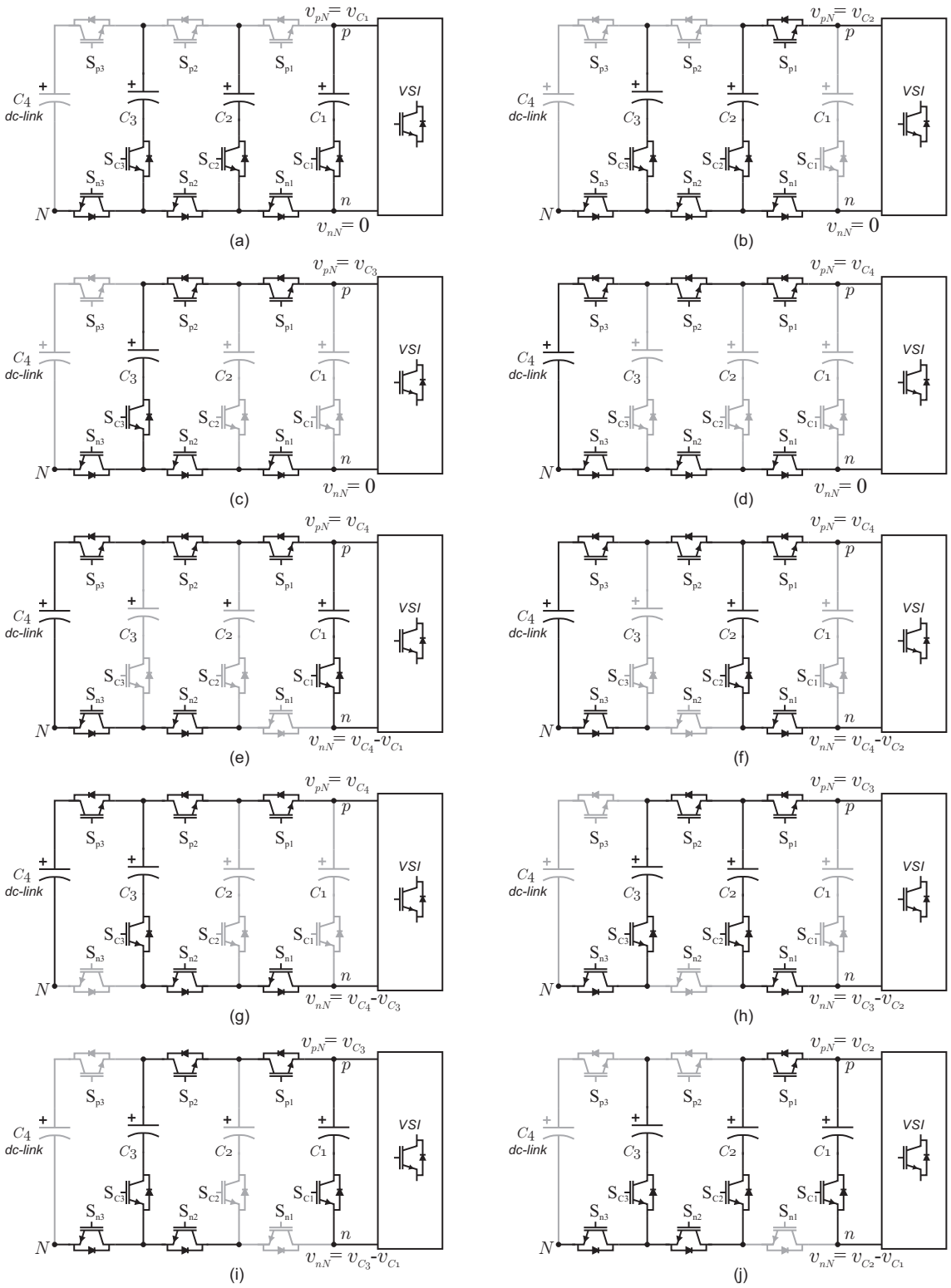


Figure 3.5. *Different DC-cell switching states (only non-redundant are shown) and their respective output potentials for a 5L-RMC.*

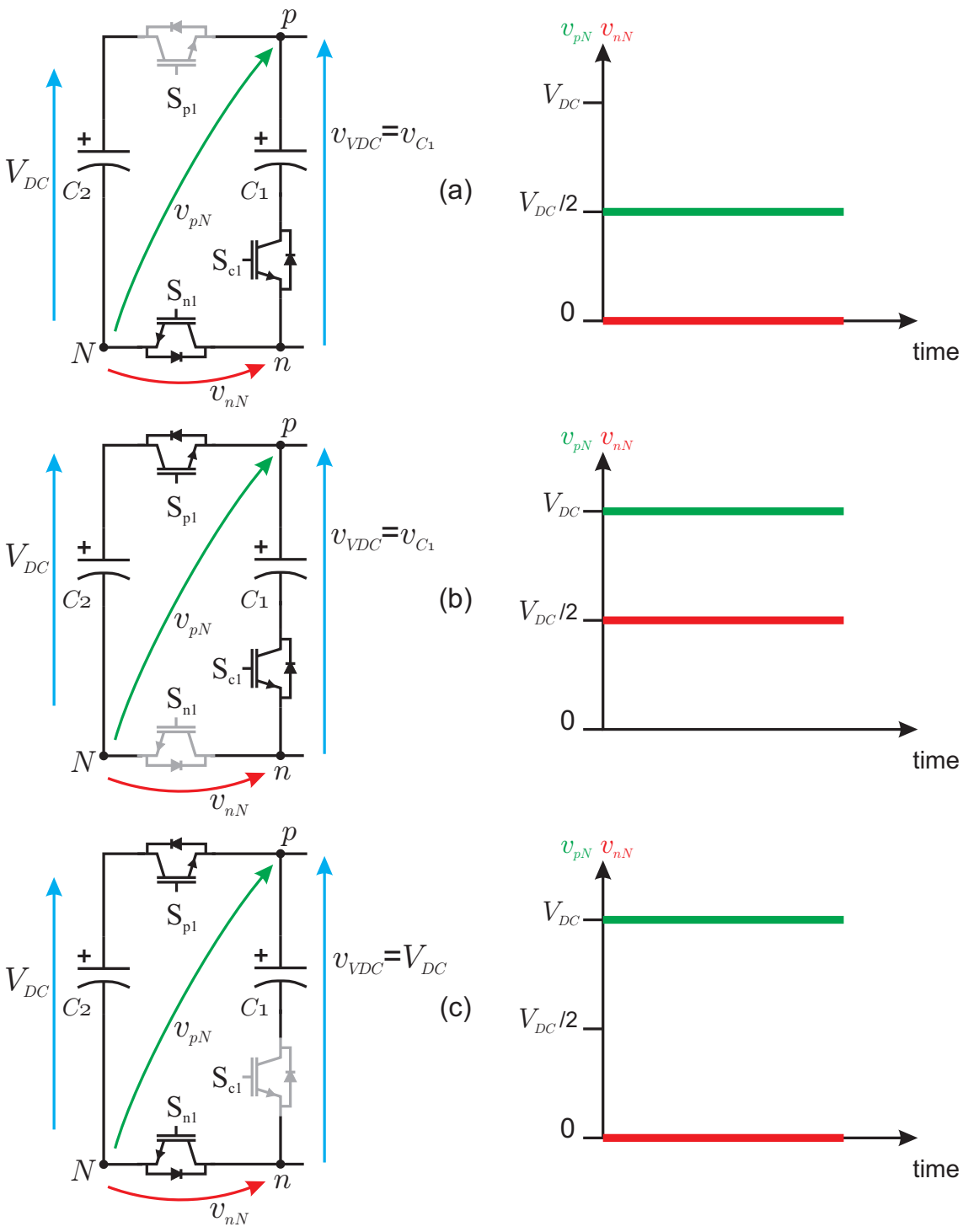


Figure 3.6. *Possible DC-DC voltage combinations in 1DC-cell RMC.*

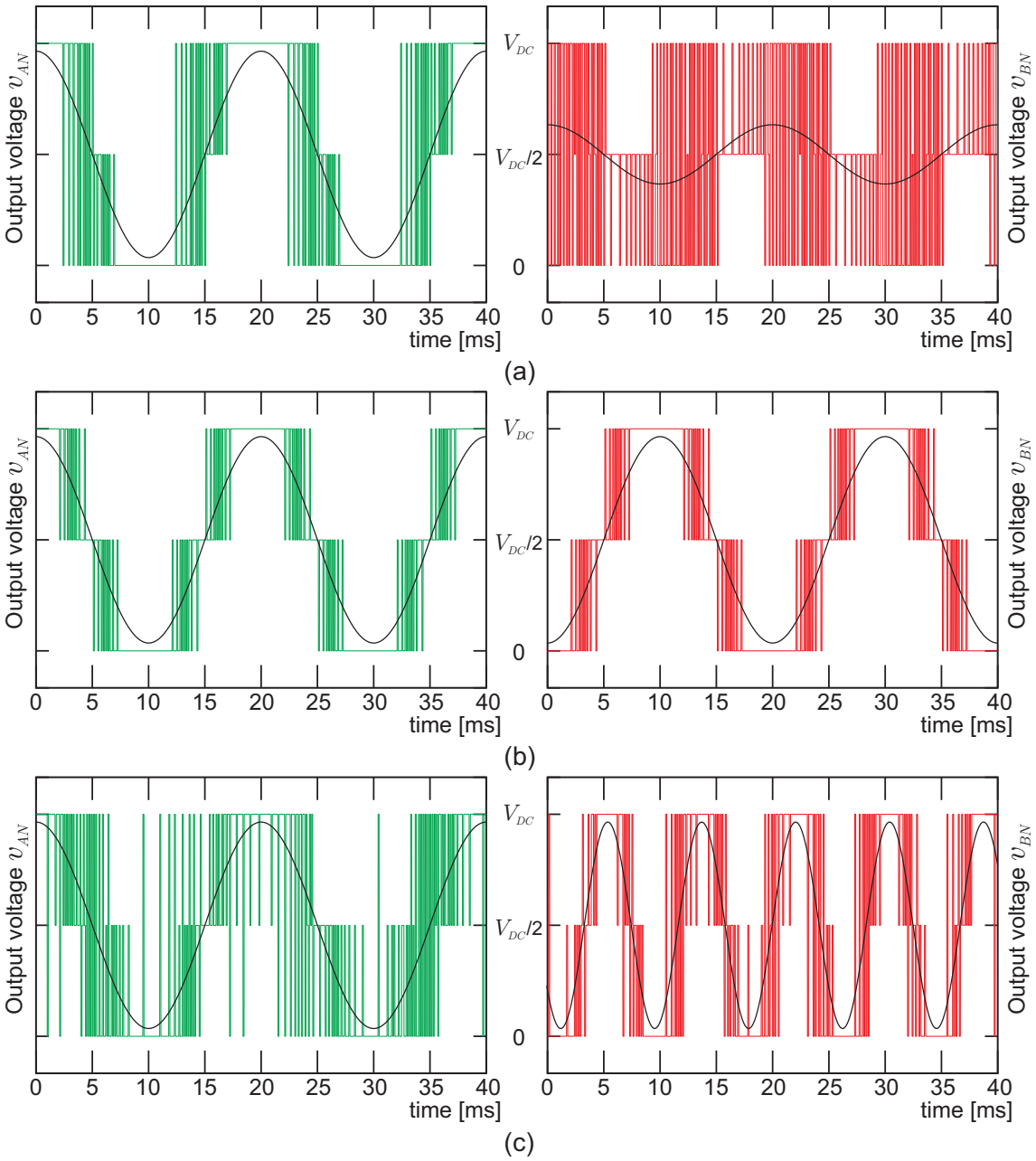


Figure 3.7. *Output voltage of the 3L-RMC: (a)* $m_A = 0{,}87$, $m_B = 0{,}3$*; (b)* $m_A = m_B = 0{,}87$ *with* $\phi_A = 0°$, $\phi_B = 180°$ *and (c)* $m_A = m_B = 0{,}87$ *with* $f_A = 50Hz$, $f_B = 120Hz$.

The 1DC-cell RMC has three power switches, all power switches can take only two possible state ON or OFF, thus the total switching states in 1DC-cell RMC is $2^3 = 8$ as is shown in Table 3.5.

It is possible see that states $S1$, $S2$, $S3$ and $S4$, are not recommended because generate an indeterminate output voltage in one or both output points. Besides that, the state S8 generate a short circuit through the flying capacitor and the source (C_2). Consequently, in the 1DC-cell RMC there are only 3 possible switching states (see Fig. 3.6).

Table 3.5
1DC-cell RMC: Switching states

State	Switching State			Output Voltage	
	S_{p1}	S_{n1}	S_{C1}	v_{pN}	v_{nN}
S1	0	0	0	indeterminate	
S2	0	0	1	indeterminate	
S3	0	1	0	indeterminate	0
S4	1	0	0	V_{DC}	indeterminate
S5	0	1	1	v_{C1}	0
S6	1	0	1	V_{DC}	v_{C1}
S7	1	1	0	V_{DC}	0
S8	1	1	1	short circuit	

From the possible switching state ($S5$, $S6$ and $S7$) it is possible to see that power switches S_{p1} and S_{n1} works in a complementary way only when power switch S_{C1} is ON.

3.2.1. Analysis of constraints

An important constraint in this topology is the voltage that the power switches need to block. The blocking voltage of the transistor in a DC-cell depends on the voltage $v^{+}_{o(k+1)} - v^{-}_{o(k+1)}$, which can change. However, there is a maximum voltage that the transistors need to block, given by:

$$\hat{v}_{block,S_{ik}} = V_{DC} - v_{Ck} \tag{3.8}$$

Where S_{ik} is the power switch i in DC-cell k for all $i \in \{p, n, C\}$, and v_{Ck} is the voltage of the capacitor in DC-cell k. In the case of the output switches (S_x, $\bar{S}_x$ with $x \in \{A, B, C\}$) the maximum blocking voltage is the full dc-link voltage.

The maximum blocking voltages of the transistors is summarized in Table 3.6.

Table 3.6
Maximum blocking voltage in RMC

$\hat{v}_{block}$	Power Switch
$\frac{V_{DC}}{4}$	S_{p3}, S_{n3}, S_{C3}
$\frac{V_{DC}}{2}$	S_{p2}, S_{n2}, S_{C2}
$\frac{3V_{DC}}{4}$	S_{p1}, S_{n1}, S_{C1}
V_{DC}	S_A, $\bar{S}_A$, S_B, $\bar{S}_B$, S_C, $\bar{S}_C$

3.2.2. Implementation in Medium Voltage

The device blocking voltage is a disadvantage, that prevents the use for medium voltage applications, thus, the scope of this topology is not for medium voltage applications. Nevertheless, multilevel converters have now been used extensively in low voltage applications, such as PV inverters, UPS systems, and wind power conversion systems (all below 690 V), and the most appropriate application is a subject of further research and exploration.

However, one solution to implement this topology in medium voltage applications is to use power semiconductors with different rating voltages for the case when is necessary block a higher voltage. Another option, is to connect additional semiconductor in series in the case where is necessary block a higher voltage.

3.2.3. Remark about the number of output level

The number of output levels in the RMC structure depends of the number of DC-cells and/or the number of output level of the DC-AC output inverter stage. For example, the 3DC-cell RMC shows in fig. 3.1 with a T-Type topology in the DC-AC output inverter stage results in a RMC topology with 9 levels instead of 5 levels. Beside that, the blocking voltage limitation will be overcome and the maximum blocking voltage will be $3V_{DC}/4$ in the power switches in the DC-cell 1.

3.3. Mathematical model

The best way to understand the behavior of a system is the mathematical description. In the case of the RMC, the equations that describe the properties of the converter are the output voltage and the inner capacitor voltage equations.

The output voltages, considered between the output point (A, B, or C in Fig. 3.1) and the neutral point of the converter N, can be expressed as a function of the switching states and inner voltages.

To find this expression there are two ways, one is using the circuits given in Fig. 3.5 considering a 2L-VSI as DC-AC stage and find an expression for each voltage. For example, the voltage in the capacitor C_1 is going to appear in the output voltage vector only if S_{C1} is ON ($S_{C1} = 1$) and $S_{p1} \neq S_x$ for $x \in \{A, B, C\}$, which can be written as:

$$v_{xN}(v_{C1}) = v_{C1} S_{C1}(S_x - S_{p1}) \tag{3.9}$$

A similar relationship can be derived for all inner voltages. For example, the voltage in C_2 is going to appear in the output voltage vector only if S_{C2} is ON and $S_{p2} \neq S_x$ if S_{C1} is OFF ($S_{C1} = 0$), but if S_{C1} is ON the condition changes to $S_{p2} \neq S_{p1}$. Equation (3.10) describes the influence of v_{C2} in the output voltage and eq. (3.11) shows the reduced expression of it.

$$v_{xN}(v_{C2}) = v_{C2}S_{C2}\big((1-S_{C1})(S_x - S_{p2}) + S_{C1}(S_{p1} - S_{p2})\big) \tag{3.10}$$
$$= v_{C2}S_{C2}\big(S_{C1}(S_{p1} - S_{p2} - S_x + S_{p2}) + (S_x - S_{p2})\big)$$
$$v_{xN}(v_{C2}) = v_{C2}S_{C2}\big(S_{C1}(S_{p1} - S_x) + (S_x - S_{p2})\big) \tag{3.11}$$

A second way to find the output voltage expression is using the possible switching states for DC-cells. The 27 possible switching states for the DC-cells are given in table 3.3, 54 considering one phase of 2L-VSI.

To determine the expression for the output voltage it is necessary to formulary expressions for all inner voltages.

For example, from Table 3.3 it is possible to see that the vectors that include v_{C1} in the output voltage are: $(-)V_2 - V_5$ (v_{nN}), $(+)V_9 - V_{10}$ (v_{pN}), $(-)V_{11} - V_{13}$ (v_{nN}), $(+)V_{17} - V_{19}$ (v_{pN}), $(-)V_{20} - V_{21}$ (v_{nN}), and $(+)V_{24} - V_{27}$ (v_{pN}). Where the symbol $-$ or $+$ represents the sign of the voltage v_{C1} in the output voltage.

The common factor in these vectors is S_{C1}. In all 18 possible voltages $S_{C1} = 1$. Furthermore, the other switching states that are constants in these vectors are S_7 and S_x.

Every time that $S_{p1} = 1$ and $S_x = 0$, $-v_{C1}$ appears in the output voltage, and when $S_{p1} = 0$ and $S_x = 1$, $+v_{C1}$ appears in the output voltage, any other combination of these switches does not generate an output voltage with v_{C1}, i.e. $S_{p1} = S_x$.

Thus, it is possible to describe the influence of v_{C1} in the output voltage by:

$$v_{xN}(v_{C1}) = v_{C1}S_{C1}(S_x - S_{p1}) \tag{3.12}$$

Following these steps it is possible find analogue expression for V_{DC}, v_{C3} and v_{C2}.

For example, for the case of V_{DC} it is possible find two big groups of output vector with this voltage: (1) when V_{DC} is generated in v_{pN} and v_{nN}, which are $V_2 - V_{11}$, V_{14}, and $V_{17} - V_{18}$, and (2) when V_{DC} is generated only in v_{pN}, which is V_1.

It is not easy to determine the common factor in this case, but in a first approximation, it is possible to discard the switching states which not present V_{DC} in the output voltages by multiplying $S_{p3}S_{C3}$. This decision reduces the output voltages with presences of V_{DC} from $V_1 - V_{11}$, V_{14}, and $V_{17} - V_{18}$ to $V_1 - V_3$, V_7, and V_9.

In these 5 switching states it is possible to see that the common factor is $(1 - S_{C3})$. This factor allow not repeat the influence of the previous switching states, but this is also the common factor of the not desired switching states (output voltage without V_{DC}) so it is necessary to be more precise to describe this voltage.

For example, by multiplying $S_{p2}S_{C2}$ when $S_{C3} = 0$ it is possible to discard the not desired switching states. This decision reduces the output voltages with presences of V_{DC} from $V_1 - V_3$, V_7, and V_9 to V_1 and V_2.

It is possible to see that the common factor in these two switching states could be $(1 - S_{C2})$. This factor allow not repeat the influence of the previous switching states, but this common factor allows the switching states V_{24}, which is a not desired switching state in this case, so it is necessary to be more precise.

V_{DC} is presents in V_1 only in v_{pN}, so one condition could be S_x to consider this switching state. This condition also considers the influence of v_{pN} in V_2 and in V_{24}. Hence, it is necessary considers now the influences of v_{nN} in V_2 and eliminates the influences of v_{pN} in V_{24}.

The common factor of V_2 and V_{24} could be $(1 - S_{C1})$ and to add the influence of v_{nN} in V_2 it is possible multiply it by the factor $(S_{p1} - S_x)$, this also eliminates the influence of v_{pN} in V_{24} and ensure the not presence of v_{nN} in V_{24}.

Thus, the influence of V_{DC} in the output voltage can be written as:

$$v_{xN}(V_{DC}) = V_{DC}\Big((1 - S_{C3})\big(S_{p2}S_{C2} + (1 - S_{C2})(S_x + S_{C1}(S_{p1} - S_x))\big) + S_{p3}S_{C3}\Big) \tag{3.13}$$

Finally, the output voltage can be expressed by the equation (3.14).

$$\begin{aligned} v_{xN} = {} & V_{DC}\Big((1 - S_{C3})\big(S_{p2}S_{C2} + (1 - S_{C2})(S_x + S_{C1}(S_{p1} - S_x))\big) + S_{p3}S_{C3}\Big) \\ & + v_{C3}S_{C3}\Big((1 - S_{C2})\big(S_{C1}(S_{p1} - S_x) + (S_x - S_{p3})\big) + S_{C2}(S_{p2} - S_{p3})\Big) \\ & + v_{C2}S_{C2}\big(S_{C1}(S_{p1} - S_x) + (S_x - S_{p2})\big) \\ & + v_{C1}S_{C1}(S_x - S_{p1}) \end{aligned} \tag{3.14}$$

Where $x \in \{A, B, C\}$, v_{C1}, v_{C2} and v_{C3} are the inner voltages of the capacitors C_1, C_2 and C_3, respectively.

These voltages can be expressed as follows as given in equations (3.15)– (3.17).

$$v_{C3} = \frac{-1}{C_3}\int \sum_{x=A}^{C} \Big(S_{C3}\Big((1 - S_{C2})\big(S_{C1}(S_{p1} - S_x) + (S_x - S_{p3})\big) + S_{C2}(S_{p2} - S_{p3})\Big)i_x\Big)\mathrm{d}t \tag{3.15}$$

$$v_{C2} = \frac{-1}{C_2}\int \sum_{x=A}^{C} \Big(S_{C2}\big(S_{C1}(S_{p1} - S_x) + (S_x - S_{p2})\big)i_x\Big)\mathrm{d}t \tag{3.16}$$

$$v_{C1} = \frac{-1}{C_1}\int \sum_{x=A}^{C} \Big(S_{C1}(S_x - S_{p1})i_x\Big)\mathrm{d}t \tag{3.17}$$

While equations (3.14)–(3.17) cover the behavior of the converter, the mathematical model of the whole system consists of converter and load equations. In this work, a passive load $L - R$ is considered, which is describe by:

$$v_{xN} = Ri_x + L\frac{\mathrm{d}i_x}{\mathrm{d}t} + v_{oN} \tag{3.18}$$

$$v_{oN} = \frac{v_{AN} + v_{BN} + v_{CN}}{3} \tag{3.19}$$

$$x \,\epsilon\, \{A, B, C\} \tag{3.20}$$

Where R and L are the load parameters and the point o is the neutral point of the three phase load.

3.4. The Classic Modulation

To implement a classic modulation in RMC is not easy. Phase-Shifted PWM or Level-Shifted PWM or a combination of both modulation strategies cannot achieve a correct modulation in all cases, even if the inner capacitor is replaced by a voltage source. Due to the switched DC-cell capacitors, there it is not straight forward to implement a carrier based PWM scheme.

However, it is possible to use a Pulse Width Modulation in a 3-phase 3-level RMC considering the following conditions:

- In a 3-phases balanced system, the sum of the three output voltage is zero, and when one output voltage is positive (or negative) the other two output voltages are negative (or positive).
- The switching state (1,1,0) for (S_{p1},S_{n1},S_{C1}) going to be used when is active a negative output voltage level and a positive output voltage level.
- The switching state (1,0,1) for (S_{p1},S_{n1},S_{C1}) going to be used when is active a positive output voltage level and the zero output voltage level.
- The switching state (0,1,1) for (S_{p1},S_{n1},S_{C1}) going to be used when is active a negative output voltage level and the zero output voltage level.

Fig. 3.8 shows the block diagram for the PWM modulation implemented in a 3-phase 3-level RMC. To understand the modulation scheme, it is a good idea separated it into two part, one for the multilevel DC-DC converter (DC-cell part) and one for the DC-AC output inverter (2L-VSI).

In a 3L-RMC with 1 DC-cell, the DC-cell PWM could be decomposed in three steps (see Fig. 3.8). In the first step is defined a new variable v_{ref}, which will be modulated to determinate the control signal for the switch S_{C1}. This new variable, v_{ref}, selects the minimum reference value between the maximum positive value and the minimum negative value, for example, if in the moment $t = k$, the references values are: $v_A^*(k) = 0{,}7$[p.u], $v_B^*(k) = -0{,}6$[p.u] and $v_C^*(k) = -0{,}1$[p.u], the value for the new variable is $v_{ref}(k) = 0{,}6$[p.u]. The second step modulates the reference signal v_{ref} using the carrier signal v_{cr1}, the output of this modulation is the signal S_{C1} and S_{p1n1}, this last signal is a new defined signal to determine when is necessary to have both switches ON, S_{p1} and S_{n1}, (1,1,0). Finally, the third step is used to determine the control signals for S_{p1} and S_{n1}, the first part of this step is used to determine which is the sign of the largest reference signal, for example, in the previous example, the sign of the largest reference signal is positive ($v_A^*(k) = 0{,}7$[p.u]) and the output of this modulation step must to be between the positive output voltage level and the zero output voltage level (1,0,1). Thus, the next block of the third step define S_{p1} and S_{n1} considering when S_{C1} is ON or OFF and if is necessary to use the positive output voltage level or the negative output voltage level.

For the 2L-VSI modulation could be decomposed in two steps (see Fig. 3.8). In the first step is defined a new variable v_{x2}^*, for all $x \in \{A, B, C\}$, this new variable is zero if

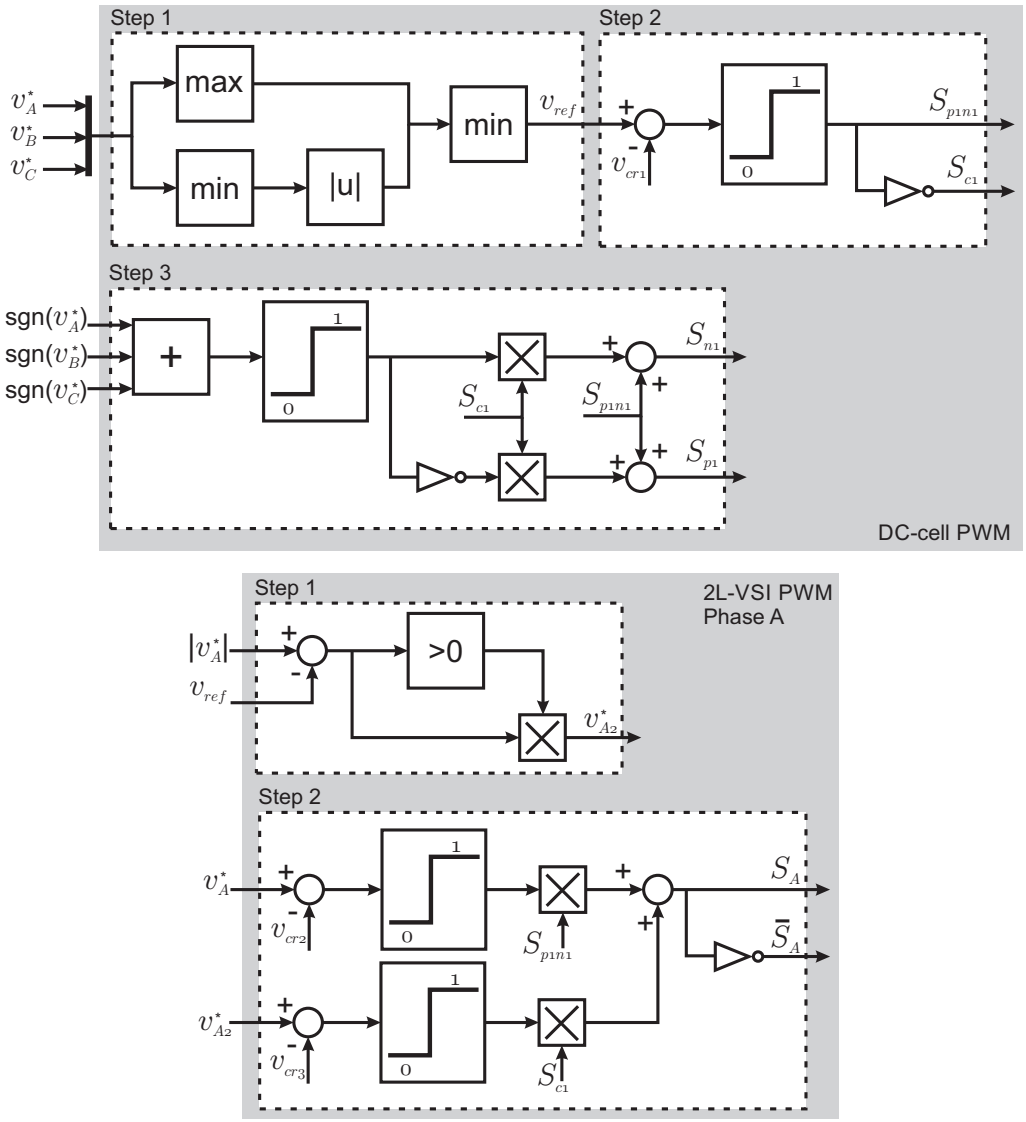


Figure 3.8. *Block diagram of PWM modulation for a 3L-RMC.*

the magnitude of the reference signal is lesser than the variable v_{ref} defined in the DC-cell modulation stage, for example, in the previous example, the reference value for the phase A is $v_A^*(k) = 0{,}7$[p.u] which is largest than $v_{ref}(k) = 0{,}6$[p.u], consequently $v_{A2}^*(k) = 0{,}1$. Finally, the second step has two part, the upper is the normal PWM for a 2L-VSI, here the reference signal v_A^* is compared with the carrier signal v_{cr2}, the output of this part is selected only when $S_{p1n1} = 1$, i.e when RMC is working as a standard 2L-VSI, the lower part of this step is the modulation of the new reference signal v_{x2}^* using the carrier signal v_{cr3}, this modulation is selected only when the active positive (or negative) output voltage and the zero output voltage could be selected (1,0,1) (or (0,1,1)).

Fig. 3.9 shows the carrier signal for the modulation, the carrier signal used to modulate the control signal S_{C1} and the carrier signal used to modulate the control signal S_A and $\bar{S}_A$ when $S_{C1} = 1$ are Phase-Shifted PWM with 180Â° shifted, see v_{cr1} and v_{cr3} in Fig. 3.9. And finally, the carrier signal used to modulate the control signal S_A and $\bar{S}_A$ when $S_{C1} = 0$ is the typical carrier signal used to modulate a 2L-VSI (see v_{cr2} in Fig. 3.9).

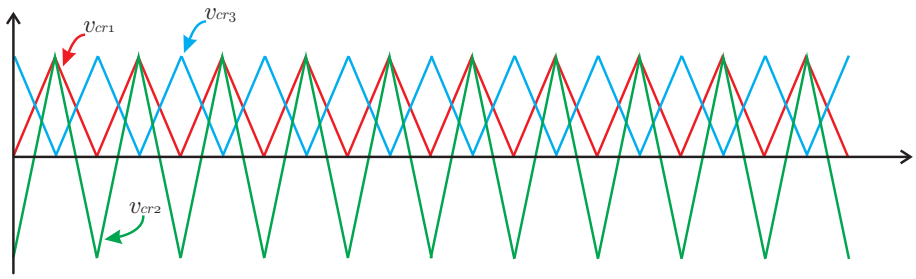


Figure 3.9. *Carrier signals in the PWM modulation for a 3L-RMC.*

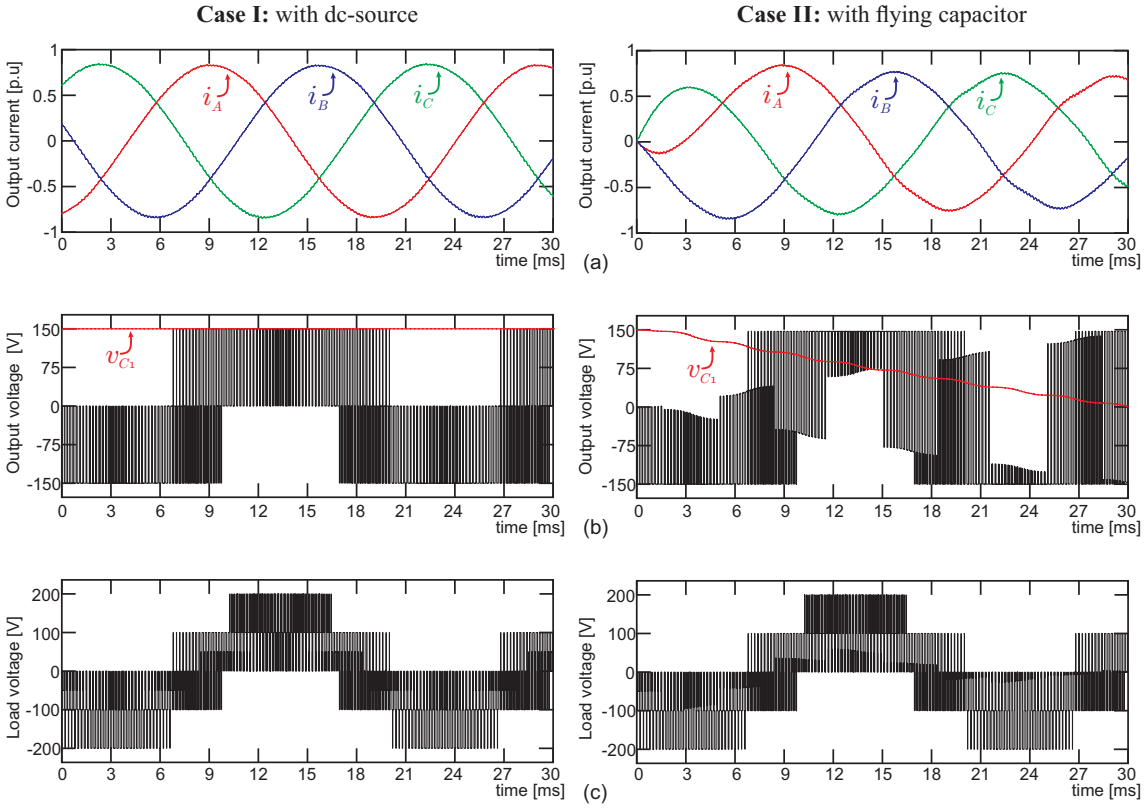


Figure 3.10. *3-phase RMC with PWM: (a) Output current; (b) Output voltage V_{AN} with inner voltage v_{C1}; (c) Load voltage V_{Ao}.*

Fig. 3.10 shows the system response of an open-loop system using PWM in a 3L-RMC. Two different cases are shown: **Case I** instead of a flying capacitor is used a dc-source to generate the inner voltage of the converter, and **Case II** is used a flying capacitor to generate the inner voltage of the converter.

In the **Case I**, the modulation strategy achieves sinusoidal output currents and 3-level output voltage (v_{AN}). In this **Case II**, however, the modulation strategy is not able to ensure a correct balanced value of the inner voltage in the flying capacitor, and as consequence of it, the flying capacitor is discharged and the 3L-RMC is now a 2L topology.

From these results, it is possible conclude that with an active control over the inner voltage in the flying capacitor (v_{C1}) could be possible to have a modulation strategy working properly even with a flying capacitor instead of a dc-source to generate the inner

voltage of the converter.

This control could be made using an injection of zero-sequence in the reference signals or a injection of third harmonic. Nevertheless, in this work was not found an appropriated control strategy over the inner voltage to solve the discharged voltage problem, and is a topic for future research.

Chapter 4

Control Strategy: Model Predictive Control

Model Predictive Control (MPC) is considered one of the most important advanced control techniques in power electronics. The MPC was proposed in the late 1970s and has since developed considerably [48–51].

In general, MPC formulates a problem of linear programming or finite quadratic programming in each sampling interval. These optimization problems can become large and the computational cost associated with solving them online can be inconvenient [52].

The term MPC does not designate a specific control strategy, but rather a wide range of control methods that employ an explicit use of a process model to obtain, through the minimization of the cost function, the control signal [49, 50].

The ideas that present, to a greater or lesser degree, all the MPC families, are basically:

- Explicit use of a model to predict the output of the process at a future time point (horizon or prediction window).
- Calculation of the control sequence for the entire prediction horizon minimizing a cost function.
- Application of only the first control signal of the obtained sequence.
- At each evaluation time, the prediction window is shifted to the future, applying only the first sequence control signal calculated at each stage, thus using a moving horizon strategy.

4.1. Classification of MPC

The MPC can be classified into at least two major categories according to the nature of the system input, EMPC (Explicit Model Predictive Control) and FCS-MPC (Finite Control Set-Model Predictive Control) [53].

4.1.1. Explicit Model Predictive Control (EMPC)

As previously mentioned, solving the optimal MPC problem requires a high computational cost, which makes it unattractive for applications that require optimum input in a few microseconds, such as in the control of power converters.

In this context, the control technique called EMPC has arisen in order to reduce the computational cost required, solving the optimal problem explicitly but off-line. To this end, EMPC considers continuous and bounded constraints of states and system inputs. Thus, it is possible to obtain a partition of the input space in n regions. The number of regions obtained depends on the number of states and inputs of the system, as well as on the prediction horizon. Therefore, for each partition it obtains an explicit solution (hence its name) for the local optimal controller of the form:

$$\kappa_i = F_i(x_k - x^*) + G_i. \tag{4.1}$$

In particular, for the so-called terminal region X_f, which is the region containing the reference, the solution is given by:

$$\kappa_f = K(x_k - x^*) + u^*, \tag{4.2}$$

Where K can be obtained analytically and u^* is the steady state input required to hold x^*. Note that this expression corresponds to a linear regulator.

Consequently, each local controller can be implemented off-line, in a table in the memory of the digital control platform. Then, in the on-line implementation, the EMPC algorithm only has to determine in which partition the system is located, $x(k)$ and thus apply the optimal input, κ_i, associated with that region.

To illustrate better how the EMPC works, an example is shown in Fig. 4.1 for a two-input system. In this case six regions have been obtained and the terminal region, X_f, has been highlighted in green, which contains the system reference $x^*[x_1^*\ x_2^*]^T$. In addition, it can be seen that the state is bounded, $x_i \in [0, x_{i\,\text{máx}}]$.

With regard to the use of EMPC for power converters, this control technique considers the duty cycle (or modulation index) as input of the system. Therefore, for this type of strategy, the input of the system belongs to a set of continuous control bounded, for example, $d_i(t) \in [0, 1]$. The cost function used considers the reference tracking error at each sampling time. Once the minimization of this error is carried out it is necessary to use a modulator to be able to control the switches of the power converter in order to apply the optimum input to the plant.

When using a PWM modulation, the typically sinusoidal actuation is compared to a high frequency triangular signal (carrier signal), generating a pulsed voltage waveform at the output of the converter. The mean value of the applied voltage, within the period of the carrier signal, corresponds to the value of the desired performance.

The EMPC performs well during steady state, as long as there are no modeling errors, so it can follow the reference without problems. The switching frequency in the EMPC is constant in the electrical variables due to the use of a traditional PWM modulator.

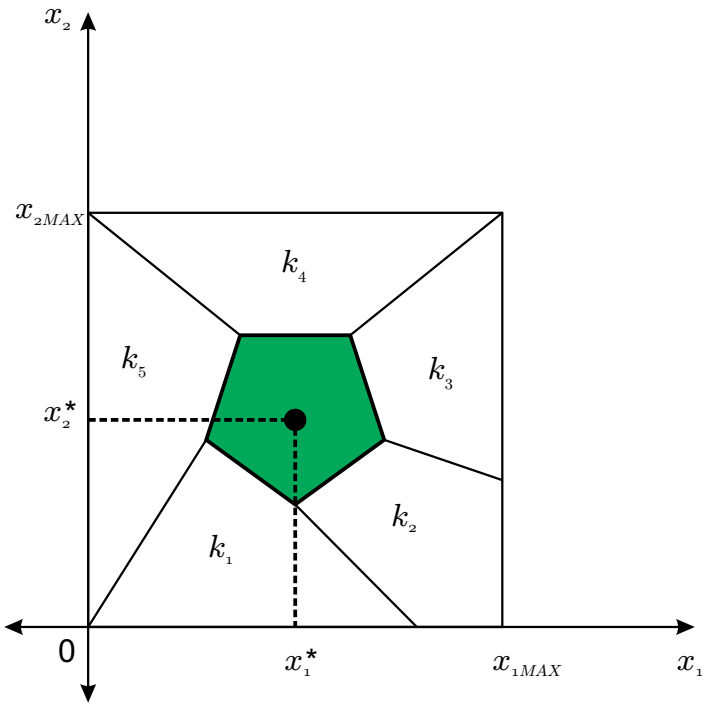


Figure 4.1. *Structure of an explicit predictive control.*

4.1.2. Finite Control Set - Model Predictive Control (FCS-MPC)

One of the most attractive predictive control formulations is the FCS-MPC [42,51,54–58], also known as direct MPC [59]. In this case, the prediction strategy directly takes into account the states of the power switches as system control inputs.

Due to, the fact that the power switches can only adopt two states, usually 1 or 0 (ON-OFF), the input is restricted to belonging to a finite set of possible combinations, hence its name FCS-MPC (Finite Control Set-Model Predictive Control). From a certain initial value of the system states, a finite number of predictions can be obtained for the different electrical variables in each sampling period, associated with the finite number of combinations of the inputs. Each of these predictions is evaluated through a cost function, applying during the following sampling period that combination of switches that minimizes this function. In this way, the predictive strategy does not require a modulation step as in the case of EMPC.

In summary, the FCS-MPC is a control technique that calculates the control action by solving, at each sampling instant, on a finite horizon, an optimal control problem based on predictions of the future behavior of the system.

Due to the characteristics presented by the FCS-MPC control strategy, it results in an easy-to-understand strategy that can be implemented, in general, to a varied set of power converters and machines, regardless of the complexity of these. FCS-MPC achieves to incorporate complex constraints and nonlinearities to the predictive model. Likewise, this predictive control technique allows, without major difficulties and choosing a correct cost function, to evaluate different minimization criteria, seeking the best performance that satisfies all of them [49,50,56,60–65].

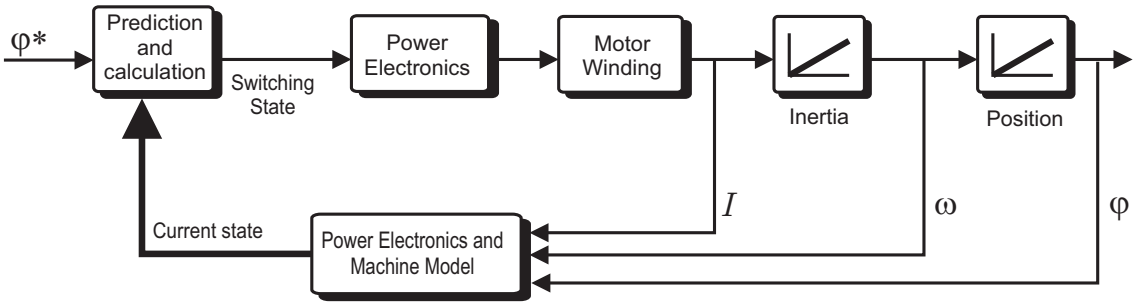


Figure 4.2. *Structure of a direct predictive control.*

Fig. 4.2 shows the typical structure of a predictive position control of a machine. The control variables of the drive, for example, machine current, velocity ω and angle φ, are entered into the model of the machine and the power electronics. The information derived from this model is given to the block called "prediction and calculation", which can be considered as the heart of the predictive control system. By comparing the current state of the machine with the reference value of the position of the drive, the correct state of the power switches that meet the optimization criterion implemented will be chosen, which, for example, can be to minimize the switching frequency, minimize current distortion or minimize ripple in torque [66].

For each switching state, the behavior of the system can be predicted so that the behavior of the inverter and the machine can be calculated in advance for each of them, allowing the calculation of the prediction [67,68].

The FCS-MPC control has shown its flexibility and good dynamic properties in power electronics, not only for controlling the waveform of the current but also in other aspects, such as commutation losses and common mode voltage reduction [69,70].

Although the FCS-MPC strategy may present certain advantages when compared to EMPC or linear control techniques, the following practical aspects should be kept in mind at the time of implementation:

- The computational effort is increased by increasing the number of switch elements (eg multilevel converters [61,65]).
- Designing the cost function, especially if it should consider more than one control goal, requires the use of weight factors. [50]
- Variation of model parameters.
- Non-zero error at steady state. [71]
- High sensitivity to measurement noise.
- The variable switching frequency of the different power semiconductors. [72]

4.2. Summary

The MPC presents a number of advantages over other methods and control strategies, among which it can highlight the following:

- The FCS-MPC is particularly attractive to engineers because no in-depth knowledge of control is required since the concepts involved are very intuitive.
- It can be used to control a wide variety of processes, from relatively simple to complex ones, including systems with long delay, non-minimal or unstable phases.
- Multivariate cases can be handled easily.
- It allows to compensate the dead times.
- It allows to follow complex references.
- It manages to compensate for the measurable disturbances by naturally incorporating the feed-forward into the control.
- In the case of unconstrained linear control systems, the resulting control is easy to implement in a linear control law.
- For linear systems with bounded constraints, the EMPC can be used to obtain a family of linear controllers for different system partitions.
- Its extension for the treatment of constraints is conceptually simple and can be included systematically during the design process.

By way of comparison, Table 4.1 summarizes the main features of both predictive control strategies, FCS-MPC and EMPC.

Table 4.1
Operating characteristics of EMPC (right) and FCS-MPC (left).

FCS-MPC	**EMPC**
Very fast response to transients.	Rapid response to transients. Faster than the linear controller but slower than FCS-MPC.
Variable switching frequency. Wide spread and variable signals spectrum.	A fixed switching frequency can be obtained, achieving a well-defined spectrum.
Non-zero error in steady state.	Good steady state performance.
It manages to face more complex objectives of control.	It is not as flexible as the FCS-MPC. It is complicated to achieve more than one goal in control.
No modulation stage required.	Modulation stage required.
Requires a model to perform prediction.	Requires an invertible model.

4.3. MPC implementation strategy

The methodology of all controls belonging to the MPC family is characterized by the strategy represented in Fig. 4.3 and detailed in the following steps:

1. The future output for a given horizon, N, called the prediction horizon, is predicted at every instant t using the system model. These predicted outputs $y(t+k,t)$ for $k = 1...N$, depend on the known values up to the instant t (previous inputs and outputs) and the future control signal $u(t+k,t)$ with $k = 0...N-1$. These control signals will be calculated and sent to the system.

2. The set of future control signals, $\vec{u} = \{u(t,t),\ldots,u(t+N-1,t)\}$, is calculated through the optimization of a certain criterion to the extent of keeping the process as close as possible to the reference trajectory, $w(t+k)$, (which can be the signal itself or a close approximation of it).These criteria generally take the form of a quadratic function of the error between the predicted output signal and the predicted reference path, $(w(t+k)-y(t+k,t))^2$, known as the cost function to be optimized (g). The control effort, in many cases, is included in the cost function. If the optimization criterion is quadratic, the model is linear and there are no restrictions, it is possible to obtain an explicit solution, in the same way as in a Linear Quadratic Regulator (LQR). Otherwise, an iterative optimization method should be employed or use *off-line* solutions such as the EMPC.

3. Only the first entry of the control sequence, $\vec{u}(t)$, this is $u(t,t)$, is sent to the process while the remaining control signals calculated, $u(t+1,t),\ldots,u(t+N-1,t)$, are discarded, because at the next sampling time $y(t+1)$ is again measured (or estimated) and step 1 is repeated with this new value and the entire control sequence $\vec{u}(t+1) = \{u(t+1,t+1),\ldots,u(t+N,t+1)\}$ is updated. Thus, $u(t+1,t+1)$ is calculated (which will initially be different from the value $u(t+1,t)$ due to the new information available) giving way to the concept of the mobile horizon.

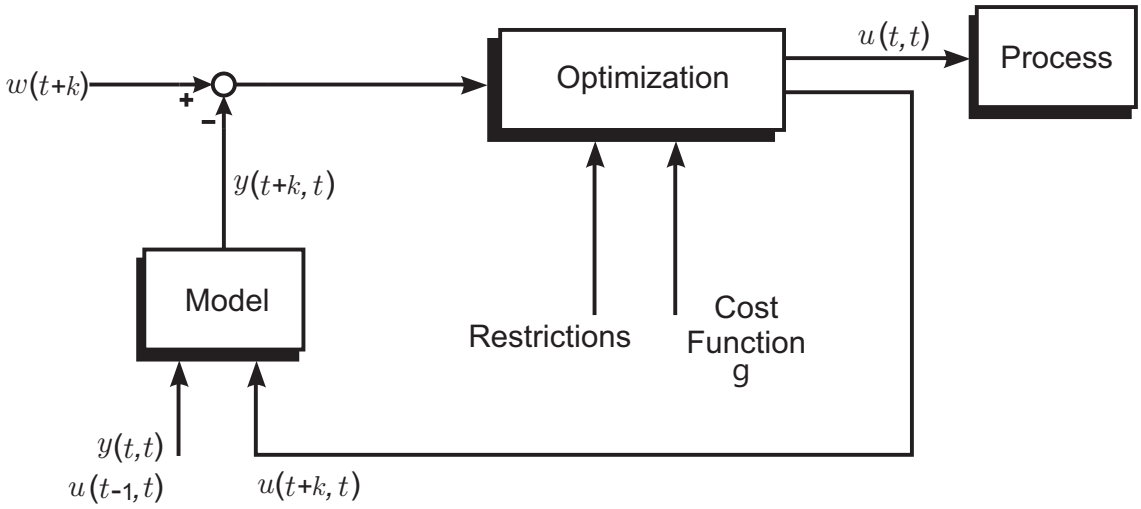


Figure 4.3. *Predictive Control Strategy.*

It is possible to make a simile between the strategy of the MPC and the control strategy used in driving an automobile. Assume a driver who knows perfectly the desired reference trajectory for a finite control horizon (for example, the journey that must be made daily from his house to his work), and taking into account the characteristics of the car decides the control action. He knows that for example, he must follow the following sequence: first accelerate, then turn left, then brake at the junction and speed up again, finally turning right and stopping at his place of work.

However, just as in a predictive control strategy, only the first control action is taken into account at each time of "*sampling*", because as in the control strategy, the driver may encounter new contingencies with each step he takes, despite knowing beforehand what would be the path "*ideal*" to follow.

For example, following the above-mentioned sequence, suppose that after accelerating (for the first time) before being able to bend in the corner a dog crosses its path, then the driver must to choice: or avoid the dog, changing the trajectory, or brake waiting for the road to clear. This is why the procedure is repeated again for the next control decision as the horizon shifts, establishing a new sequence of actions to follow based on the events given at each sampling time.

4.4. FCS-MPC applied to the Reduced Multilevel Converter

There is not a simple modulation scheme that can manage the inner voltages of the converter and ensure a correct balancing of the capacitors voltages in an open loop control strategy. For this reason, the most simple control strategy that allows to handle multiple control objectives without a modulation stage is FCS-MPC.

MPC strategies operate in discrete time with a fixed sampling frequency $f_s = T_s^{-1}$, thus it is necessary to obtain a discrete time model of the whole system, converter and load, eq. (3.14) − (3.20). To obtain this model of the RMC converter described in Chapter 3, first, the three inner voltages and the output current are considered as system states. This is:

$$x(k) = [v_{C3}(k)\ v_{C2}(k)\ v_{C1}(k)\ i_A(k)\ i_B(k)\ i_C(k)]^T \tag{4.3}$$

$$u(k) = [S_1\ S_2\ S_3\ S_4\ S_5\ S_6\ S_7\ S_8\ S_9\ S_A\ S_B\ S_C]^T \tag{4.4}$$

Where the equation (4.3) represents the system states and the equation (4.4) represents the control outputs. Therefore, equations (3.14) − (3.20) can be discretized using the forward Euler method and rewritten for an FCS-MPC control strategy such as:

$$
\begin{aligned}
v_{xN}^{k+1} = V_{DC}\Big(\Big(1 - S_{C3}^k\Big) \Big(S_{C2}^k S_{p2}^k + \Big(1 - S_{C2}^k\Big) \Big(S_{C1}^k \Big(S_{p1}^k - S_x^k \Big) + S_x^k \Big) \Big) + S_{p3}^k S_{C3}^k \Big) \\
+ \mathbf{v}_{C3}^k S_{C3}^k \Big(\Big(1 - S_{C2}^k\Big) \Big(S_{C1}^k \Big(S_{p1}^k - S_x^k \Big) + \Big(S_x^k - S_{p3}^k \Big) \Big) + S_{C2}^k \Big(S_{p2}^k - S_{p3}^k \Big) \Big) \\
+ \mathbf{v}_{C2}^k S_{C2}^k \Big(\Big(S_x^k - S_{p2}^k \Big) + S_{C1}^k \Big(S_{p1}^k - S_x^k \Big) \Big) \\
+ \mathbf{v}_{C1}^k S_{C1}^k \Big(S_x^k - S_{p1}^k \Big)
\end{aligned} \tag{4.5}
$$

$$
v_{oN}^{k+1} = \frac{v_{AN}^{k+1} + v_{BN}^{k+1} + v_{CN}^{k+1}}{3} \tag{4.6}
$$

$$
i_x^{k+1} = H_1 \mathbf{i}_x^k + H_2 \Big(v_{xN}^{k+1} - v_{oN}^{k+1} \Big) \tag{4.7}
$$

$$
v_{C1}^{k+1} = \mathbf{v}_{C1}^k - \sum_{x=A}^{C} \Big(\frac{T_s}{2C_1} \Big(i_x^{k+1} + \mathbf{i}_x^k \Big) \Big(S_{C1}^k \Big(S_x^k - S_{p1}^k \Big) \Big) \Big) \tag{4.8}
$$

$$
v_{C2}^{k+1} = \mathbf{v}_{C2}^k - \sum_{x=A}^{C} \Big(\frac{T_s}{2C_2} \Big(i_x^{k+1} + \mathbf{i}_x^k \Big) \Big(S_{C2}^k \Big(\Big(S_x^k - S_{p2}^k \Big) + S_{C1}^k \Big(S_{p1}^k - S_x^k \Big) \Big) \Big) \Big) \tag{4.9}
$$

$$
\begin{aligned}
v_{C3}^{k+1} = \mathbf{v}_{C3}^k - \sum_{x=A}^{C} \Big(\frac{T_s}{2C_3} \Big(i_x^{k+1} + \mathbf{i}_x^k \Big) \Big(S_{C3}^k \Big(\Big(1 - S_{C2}^k\Big) \Big(S_{C1}^k \Big(S_{p1}^k - S_x^k \Big) \\
+ \Big(S_x^k - S_{p3}^k \Big) \Big) + S_{C2}^k \Big(S_{p2}^k - S_{p3}^k \Big) \Big) \Big) \Big)
\end{aligned} \tag{4.10}
$$

$$
x \in \{A, B, C\} \tag{4.11}
$$

Where $\mathbf{v}_{C3}^k$, $\mathbf{v}_{C2}^k$, $\mathbf{v}_{C1}^k$ and $\mathbf{i}_x^k$ denote the measured values of the inner voltages and the output current at the instant k, being:

$$
\begin{aligned}
H_1 &= \mathrm{e}^{-T_s \frac{R}{L}} \\
H_2 &= \frac{1}{R}(1 - H_1)
\end{aligned}
$$

With T_s the sampling period used.

The equations (4.5), (4.10), (4.9) and (4.8) present multiplications of states by inputs, which makes the whole system nonlinear.

In addition to the clear nonlinearity present, the computational cost to calculate the output using the FCS-MPC control strategy is quite high, in the case of 5-level 3-phase RMC, there are 216 possible switching states which should be evaluated, see eq. (3.3).

In the proposed topology, the control objectives are the balancing of inner capacitor voltages and the control of the output currents. As discussed in Chapter 3 in Section 3.2, for a $4:3:2:1$ ratio, the reference for the internal voltages of the RMC converter are:

$$
v_{C1}^* = \frac{V_{DC}}{4} \quad , \quad v_{C2}^* = \frac{V_{DC}}{2} \quad \textit{and} \quad v_{C3}^* = 3\frac{V_{DC}}{4}
$$

To incorporate all control objectives, the error signal is defined as:

$$e(k) \triangleq \begin{bmatrix} v_{C1}^*(k) - v_{C1}(k) \\ v_{C2}^*(k) - v_{C2}(k) \\ v_{C3}^*(k) - v_{C3}(k) \\ i_A^*(k) - i_A(k) \\ i_B^*(k) - i_B(k) \\ i_C^*(k) - i_C(k) \end{bmatrix} \tag{4.12}$$

A prediction horizon $N = 1$ has been established, defining the cost function as:

$$\begin{aligned} g^{k+1} = &\left(i_A^* - i_A^{k+1}\right)^2 + \left(i_B^* - i_B^{k+1}\right)^2 + \left(i_C^* - i_C^{k+1}\right)^2 \\ &+\lambda_1 \left(v_{C1}^* - v_{C1}^{k+1}\right)^2 + \lambda_2 \left(v_{C2}^* - v_{C2}^{k+1}\right)^2 + \lambda_3 \left(v_{C3}^* - v_{C3}^{k+1}\right)^2 \end{aligned} \tag{4.13}$$

Where λ_1, λ_2 and λ_3 are weighting factors which determine the relative importance of the respective errors. These weighting factors are calculated in function of the normalized value of the variables.

Although the analytical solution to this problem is not trivial, an optimal system input can easily be obtained by evaluating all possible combinations of S_i in the cost function (4.13). Finally, the combination of switches S_i which minimizes (4.13) of the analyzed model is applied during the next sampling period.

Fig. 4.4 shows the block diagram for the FCS-MPC strategy. Where (1) represents the block of the estimation and predictions stage of the control strategy; (2) represents the cost function evaluation considering all 216 possible state, the equation for g is given in eq. (4.13); and finally, (3) represents the power circuit, with the measurements of the inner voltages in the converter and the output currents in the load.

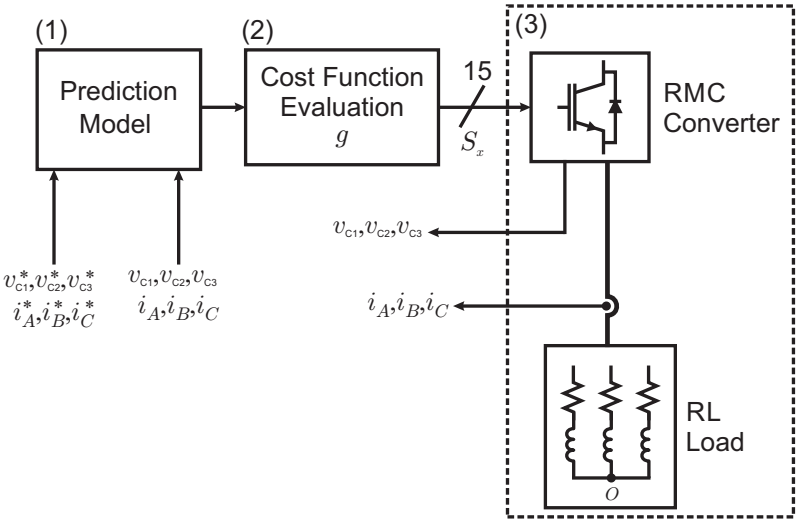


Figure 4.4. *Control scheme for FCS-MPC.*

Chapter 5

RMC: Analysis and Performance

To verify the behavior and the performance of the proposed topology, the RMC 3-level and 5-level topology will be simulated. The simulation is carried out using the software PLECS® .

The simulation results will be compared with commercial topologies, for the case of 3-level topology, RMC will be compared with the NPC (chapter 2, section 2.1) and SMC of 1 cell 2 stacks, which is known as the T-Type converter (chapter 2, section 2.4). And for the case of 5-level topology, RMC will be compared with the ANPC (chapter 2, section 2.2) and SMC of 2 cells 2 stacks.

The comparison will be done considering different aspects that could be cataloged in two big groups: the response of the system and the characteristics of the structure.

The principal points considered in both categories are described below.

System Response:

- Output currents
- Output voltages (v_{xN})
- Capacitor voltage balance
- Harmonic spectrum for output voltage and output current
- Total Harmonic Distortion
- Dynamic characteristic

Characteristics of the structure:

- Blocking voltage
- Switching frequency
- Switching and conduction losses
- Storage energy and size of the inner capacitors

5.1. System Response

Since the proposed converter has not a modulation stage that allows balancing the inner voltage, the control strategy used will be FCS-MPC (chapter 4).

In order to have a fair comparison, in spite of the commercial topologies analyzed have a well-studied modulation stage, all topologies simulated in this section will be controlled by FCS-MPC changing the cost function in function of the specific requirements of the different topologies.

The circuit analyzed considers the converter and a passive load (RL). Since the RMC has a blocking voltage limitation (see chapter 3 subsection 3.2.1) the dc-link voltage is set to 700V. For the FCS-MPC strategy, a 10kHz sampling frequency is enough high to ensure that the performance of the control strategy will be acceptable and the differences between the system responses could be attributed to the converter topology instead of the control strategy. The most relevant parameters of the converter and control are detailed in Table 5.1.

Table 5.1
Simulation parameters

Parameter	Value
Voltage *dc-link*	700 V
Load Resistance	16 Ω
Load Inductance	30 mH
Inner Capacitors	330 μF
Sampling period	100 μs

5.1.1. 3-Level Topologies

5.1.1.a. Cost Function Definition

The cost function for RMC is defined by the equation:

$$g^{k+1} = \left(i_A^* - i_A^{k+1}\right)^2 + \left(i_B^* - i_B^{k+1}\right)^2 + \left(i_C^* - i_C^{k+1}\right)^2 + \lambda \left(v_{C1}^* - v_{C1}^{k+1}\right)^2 \tag{5.1}$$

The cost function for NPC and T-type converter are the same and defined by equation (5.2):

$$g^{k+1} = \left(i_A^* - i_A^{k+1}\right)^2 + \left(i_B^* - i_B^{k+1}\right)^2 + \left(i_C^* - i_C^{k+1}\right)^2 + \lambda_1 \left(\left(v_C^* - v_{C1}^{k+1}\right)^2 + \left(v_C^* - v_{C2}^{k+1}\right)^2\right) \tag{5.2}$$

Where v_{C1}^* in equation (5.1) is the reference value for the inner voltage of the converter and the variable v_C^* in equation (5.2) is the reference value for the dc-link capacitor voltages. The weighting factor λ_1 is calculated in function of the normalized value of the variables.

5.1.1.b. Simulation Results

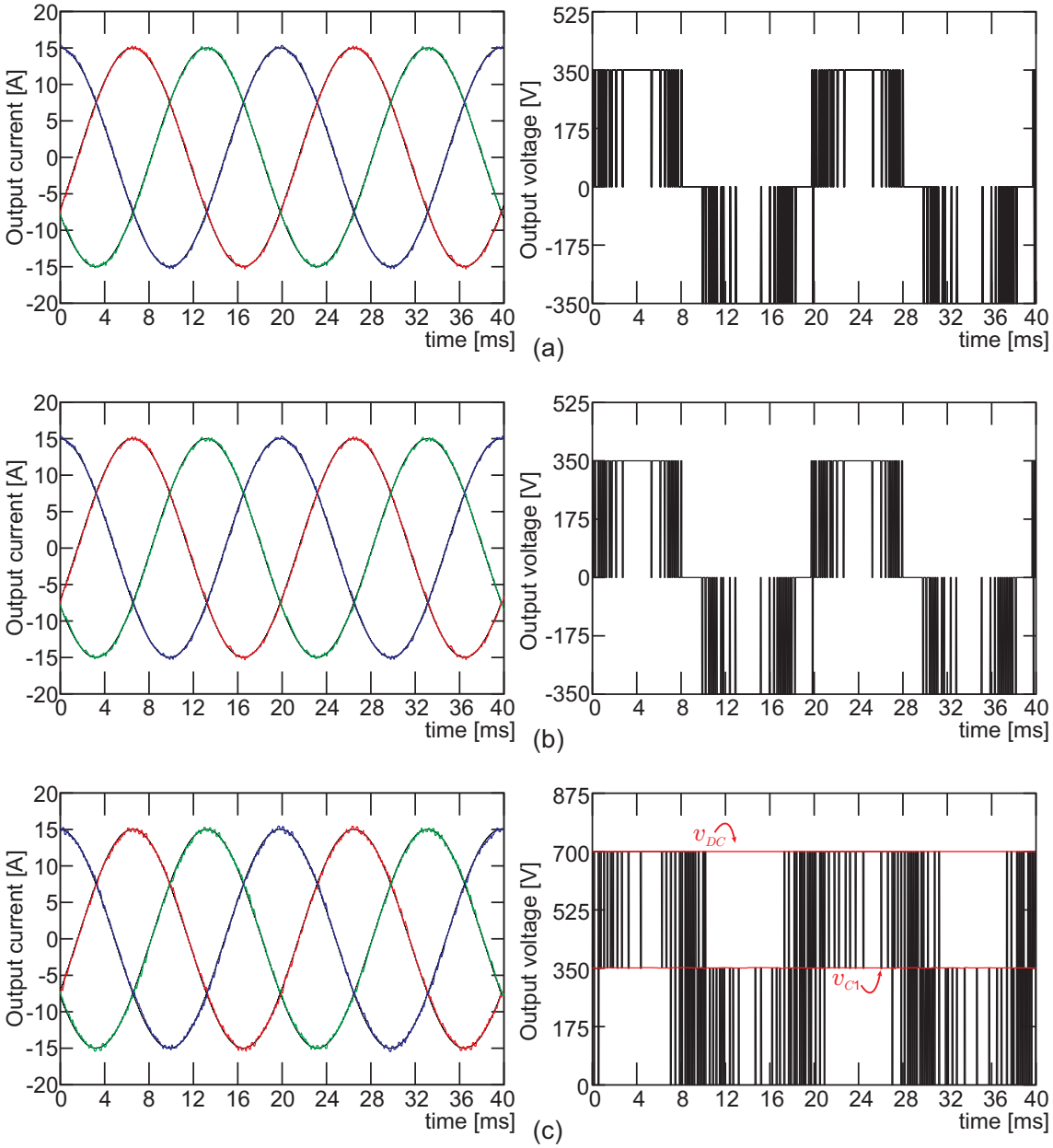


Figure 5.1. *Output currents and output voltage (v_{AN}). Steady-state for $\hat{i} = 15A$: (a) NPC converter; (b) T-type converter; (c) RMC converter.*

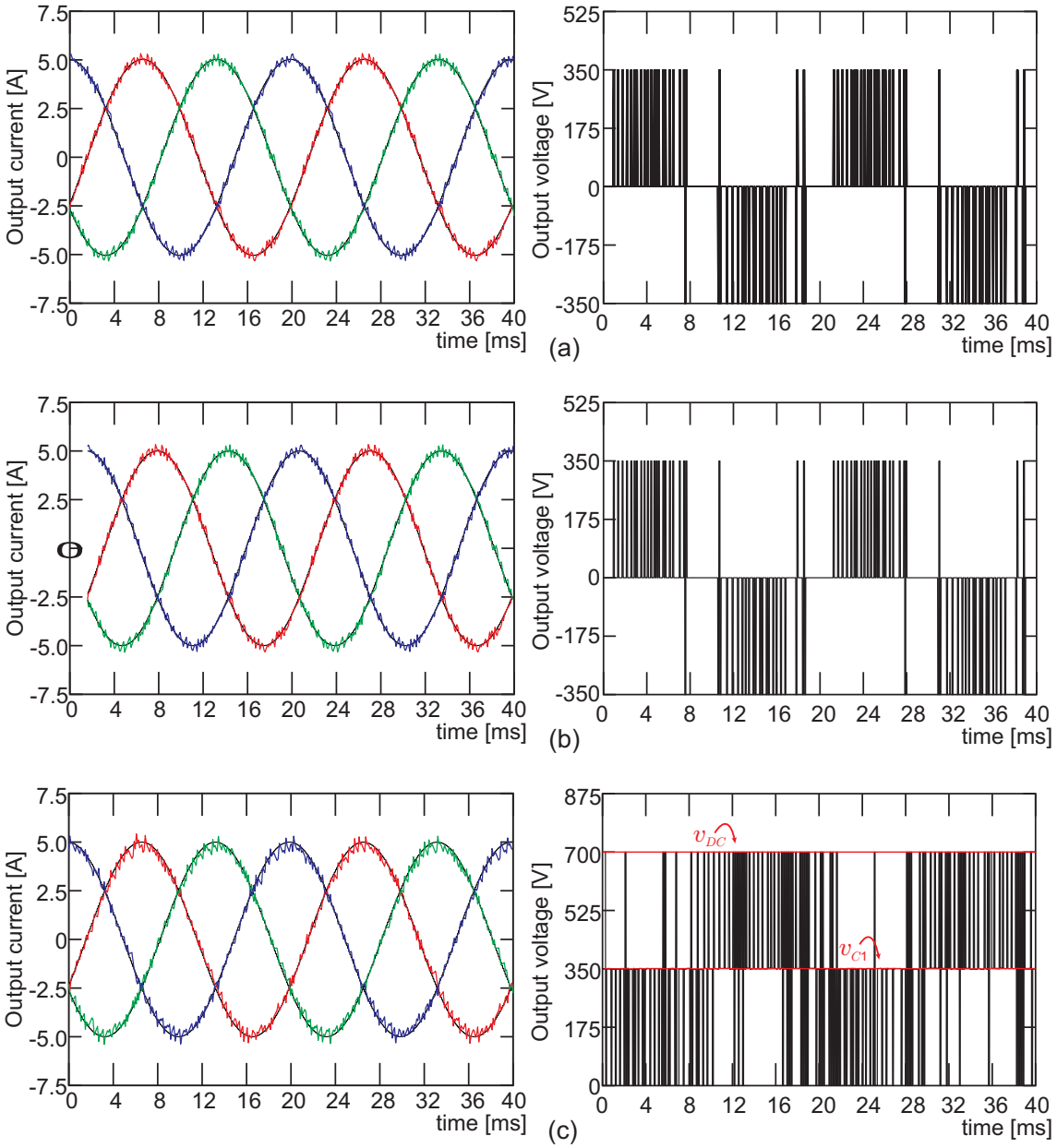


Figure 5.2. *Output currents and output voltage (v_{AN}). Steady-state for $\hat{i} = 5A$: (a) NPC converter; (b) T-type converter; (c) RMC converter.*

Fig. 5.1 and Fig. 5.2 show the steady-stay behavior of the system with 3-level topologies for two different operation points. Fig. 5.1 shows the steady-stay for an output current reference of 97 %I_{nom} and Fig. 5.2 shows the output variables for an output current reference of 32 %I_{nom}.

The NPC and T-type converter (Fig. 5.1-(a),(b) and Fig. 5.2-(a),(b)) achieve a sinusoidal waveform in the output currents with a maximum current ripple of 1.1 % of the nominal value.

The RMC topology (Fig. 5.1-(c)), also achieve a sinusoidal waveform in the output currents, but presents a higher ripple in the current than NPC and T-type converters,

which is 1.8 % of the nominal value, this difference in the output current is a consequence of the output voltage, which has a higher switching frequency than NPC or T-type converter. Switching frequency in the output voltage is 5200Hz for RMC and 4800Hz for NPC and T-type, in both cases the switching frequency is calculated as the average of the number of commutations in one period of the fundamental.

However, the three converters balanced the capacitor voltages and achieve three level output voltage in both operation points. Beyond that, the Total Harmonic Distortion (THD) for the output current and output voltage is shown in Table 5.2, and it is possible to see in these results that there are not big differences between the RMC, NPC and the T-type topology, so the performance of the RMC is comparable to the NPC and T-type, it is not really best or worst, but these results show that the 3L-RMC works.

Table 5.2
THD for 3-level topologies

Topology	**Current THD**		**Voltage THD**	
	15A	5A	15A	5A
NPC	1.32 %	4.03 %	48.4 %	54.3 %
T-type	1.32 %	4.02 %	48.3 %	54.8 %
RMC	1.55 %	4.31 %	48.8 %	55.2 %

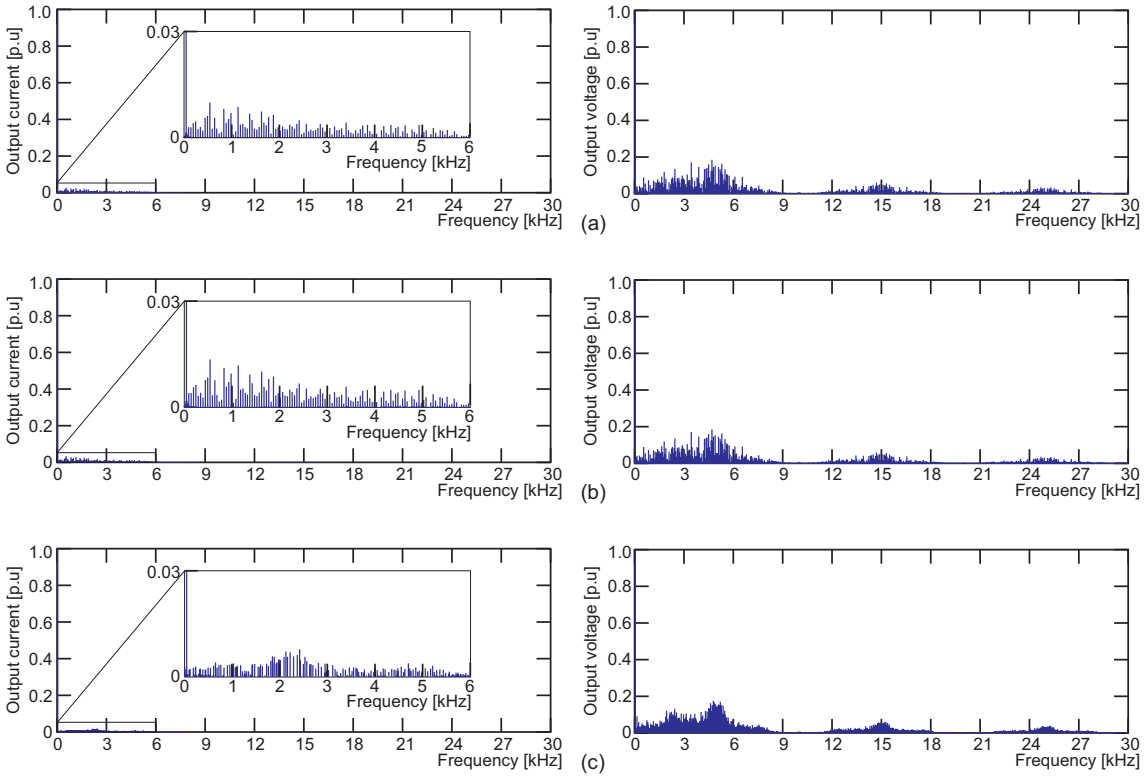


Figure 5.3. *Output currents and output voltage (v_{AN}) spectrum, for $\hat{i} = 15A$: (a) NPC converter; (b) T-type converter; (c) RMC converter.*

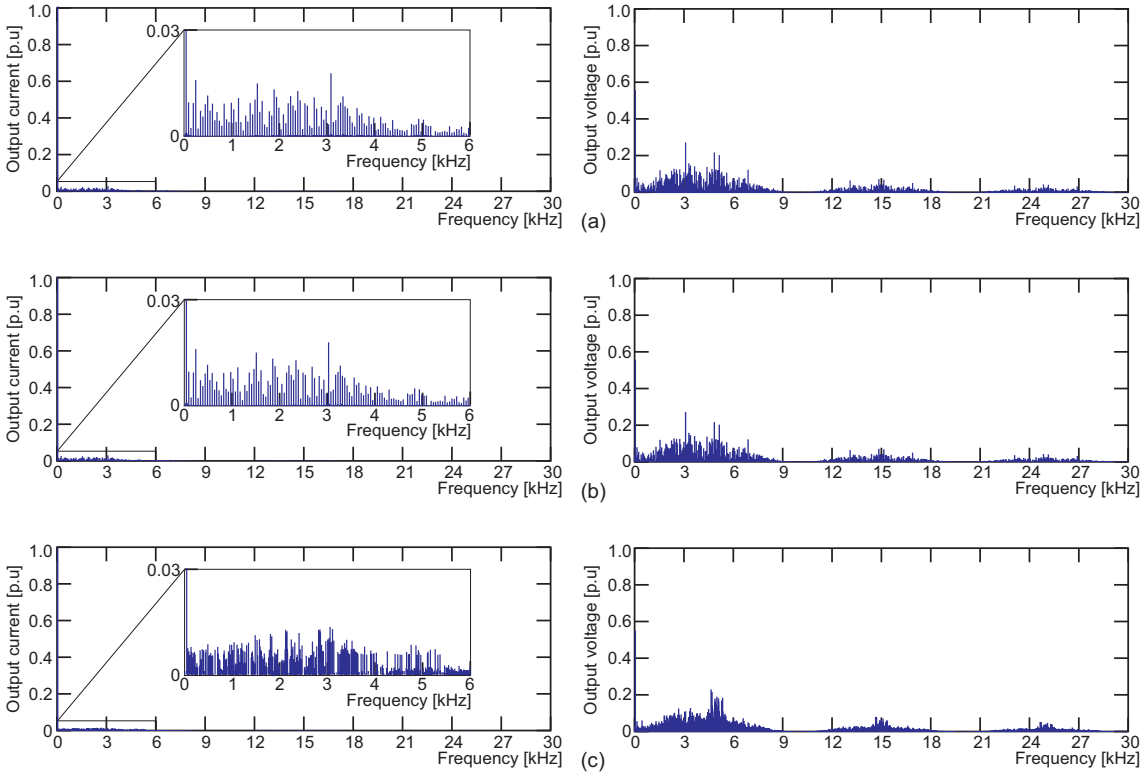


Figure 5.4. *Output currents and output voltage (v_{AN}) spectrum, for $\hat{i} = 5A$: (a) NPC converter; (b) T-type converter; (c) RMC converter.*

Fig. 5.3 and Fig. 5.4 show the harmonic spectrum for the output current and output voltage in phase A. The current spectrums show the characteristic spectrum of a FCS-MPC controller, which has a widespread spectrum and changes significantly for the different operation points. However, in the output voltage spectrum, the harmonics are concentrated around the frequency 5kHz and its multiples, being 5kHz the half of the sampling frequency.

Finally, to verify the dynamic behavior of the system, Fig. 5.5 shows the system response after a step in the current references, from $\hat{i}_X = 15$A to $\hat{i}_X = 5$A with a phase shift of 180°. In this case, the NPC converter takes 2.18ms to achieve the new value, the T-type converter 2.19ms and the RMC converter 2.18ms. All 3L converters, do not present a big perturbation in the output current during the transient, which is a characteristic of the dynamic response of the FCS-MPC, and the type of topology used does not have a big impact in this performance. In addition, in the case of RMC, the control of the inner voltage is fast enough to ensure no perturbation in the desired value of the flying capacitor voltage of the converter.

A remark of these results is that RMC topology works in both cases, steady-state and dynamic performance, and its results are quite comparable with another 3 level inverters considering same control strategy and load.

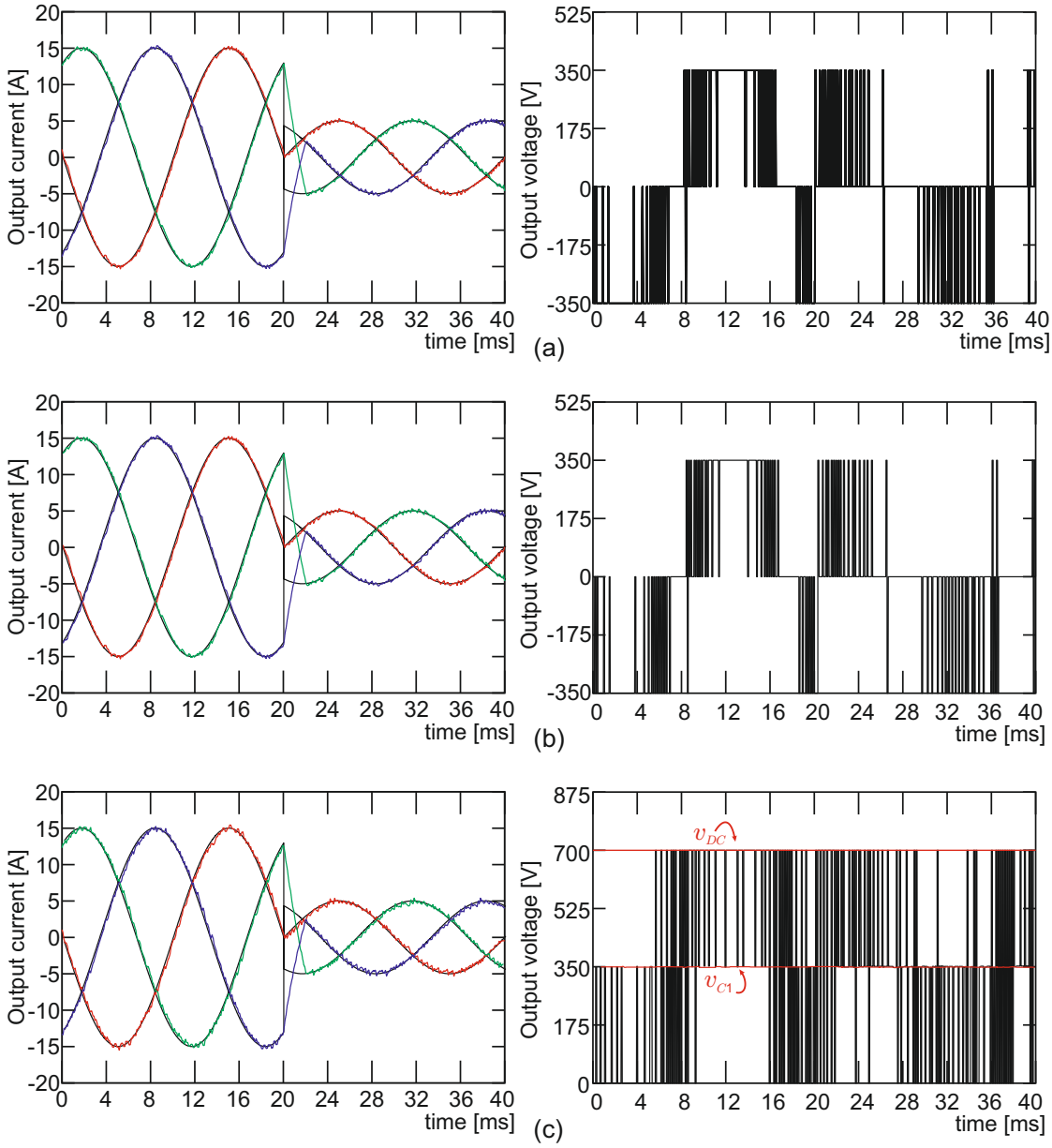


Figure 5.5. *Output currents and output voltage (v_{AN}). Dynamic response: (a) NPC converter; (b) T-type converter; (c) RMC converter.*

5.1.2. 5-Level Topologies

5.1.2.a. Cost Function definition

The cost function for RMC is defined by the equation (4.13) (chapter 4).

For the case of ANPC, the cost function needs to add the term for the inner voltage of C_{1X} and is defined by the equation:

$$\begin{aligned} g^{k+1} = &\left(i_A^* - i_A^{k+1}\right)^2 + \left(i_B^* - i_B^{k+1}\right)^2 + \left(i_C^* - i_C^{k+1}\right)^2 \\ &+\lambda_1 \left(\left(v_{C1}^* - v_{C1A}^{k+1}\right)^2 + \left(v_{C1}^* - v_{C1B}^{k+1}\right)^2 + \left(v_{C1}^* - v_{C1C}^{k+1}\right)^2 \right) \end{aligned} \tag{5.3}$$

Where v_{C1}^* is the reference value for the inner voltage of the converter and λ_1 is the weighting factor and is calculated in function of the normalized value of the variables.

For the case of SMC, the cost function needs to add the term for the inner voltage of C_{1E1} and C_{1E2}, and is defined by the equation:

$$\begin{aligned} g^{k+1} = &\left(i_A^* - i_A^{k+1}\right)^2 + \left(i_B^* - i_B^{k+1}\right)^2 + \left(i_C^* - i_C^{k+1}\right)^2 \\ &+\lambda_1 \left(\left(v_{C11}^* - v_{C11A}^{k+1}\right)^2 + \left(v_{C11}^* - v_{C11B}^{k+1}\right)^2 + \left(v_{C11}^* - v_{C11C}^{k+1}\right)^2 \right) \\ &+\lambda_2 \left(\left(v_{C12}^* - v_{C12A}^{k+1}\right)^2 + \left(v_{C12}^* - v_{C12B}^{k+1}\right)^2 + \left(v_{C12}^* - v_{C12C}^{k+1}\right)^2 \right) \end{aligned} \tag{5.4}$$

Where v_{C11}^* and v_{C12}^* are the reference value for the inner voltages of the converter and $\lambda_1 = \lambda_2$ are the weighting factors and are calculated in function of the normalized values, i.e $\lambda_1 = I_{nom}/V_{C_{nom}}$.

5.1.2.b. Simulation Results

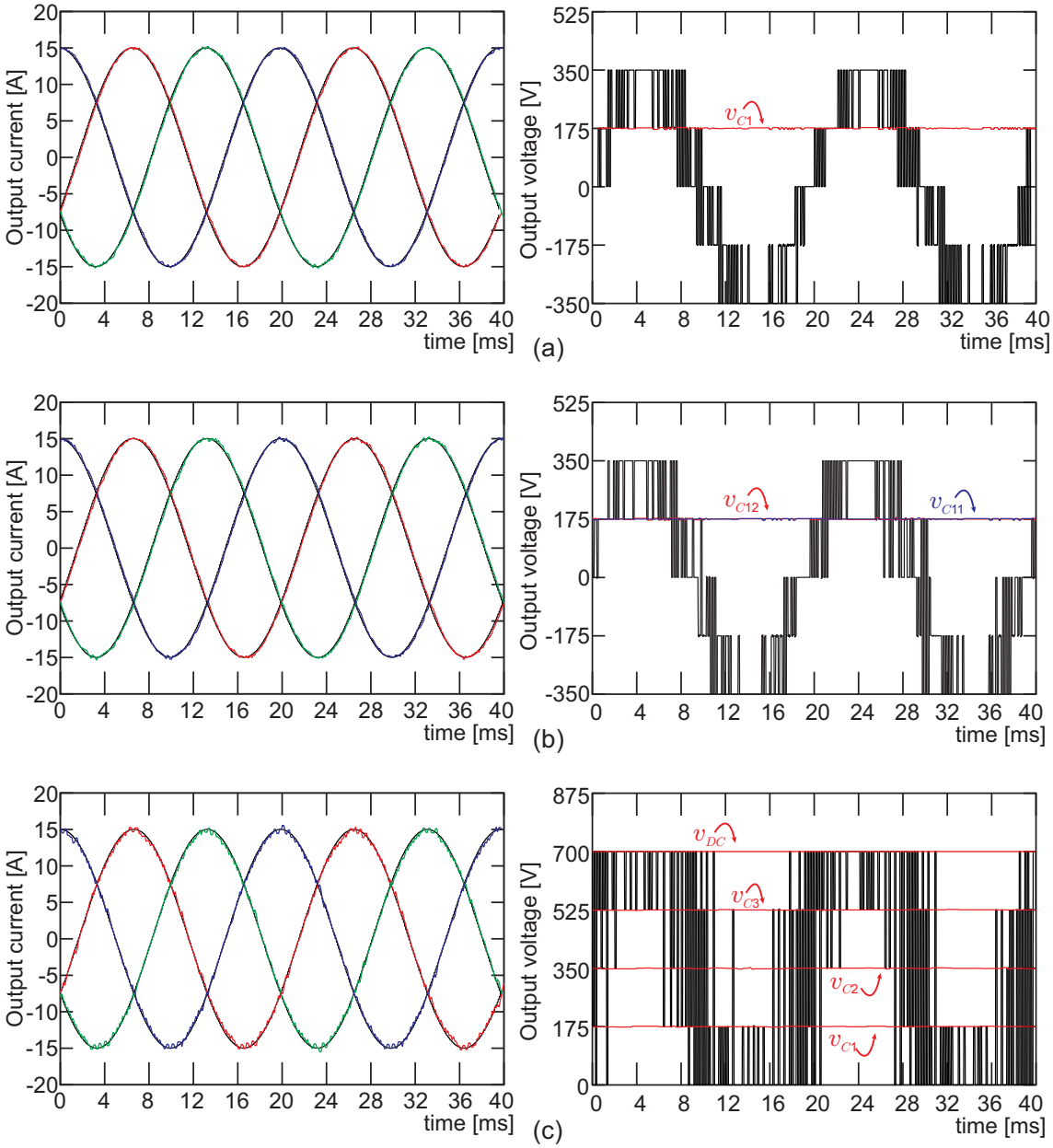


Figure 5.6. *Output currents and output voltage (v_{AN}). Steady-state for $\hat{i} = 15A$: (a) ANPC converter; (b) SMC converter; (c) RMC converter.*

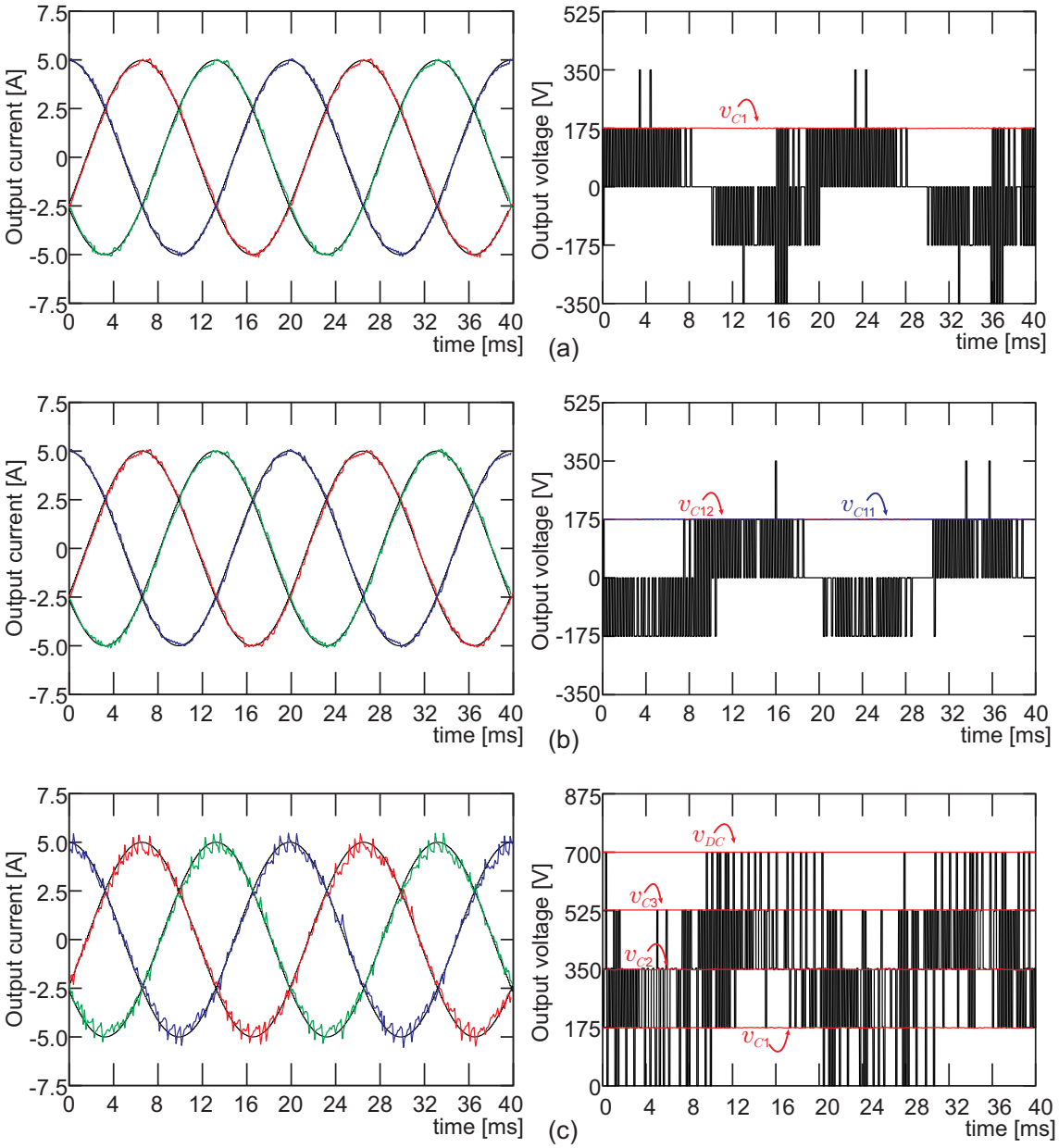


Figure 5.7. *Output currents and output voltage (v_{AN}). Steady-state for $\hat{i} = 5A$: (a) ANPC converter; (b) SMC converter; (c) RMC converter.*

Fig. 5.6 and Fig. 5.7 show the steady-stay behavior of the system with 5-level topologies for two different operation point. Fig. 5.6 shows the steady-stay for an output current reference of 97 %I_{nom} and Fig. 5.7 shows the output variables for an output current reference of 32 %I_{nom}.

The ANPC and SMC converter (Fig. 5.6-(a),(b) and Fig. 5.7-(a),(b)) achieve a sinusoidal waveform in the output currents with a maximum current ripple of 0.8 % of the nominal value. The RMC topology (Fig. 5.6-(c)), also achieve a sinusoidal waveform in the output currents, but the ripple in the output current is 1.1 % of the nominal value for high reference values and 2.05 % for low reference values. Since the 5L-RMC has less

switching states than ANPC or SMC, the FCS-MPC has less options to choose, and as a consequence, RMC presents a higher ripple in the output currents.

The switching frequency in the output voltage of ANPC and SMC converter is 3900Hz and for RMC is 4050Hz, the switching frequency is calculated as the average of the number of commutations in one period of the fundamental.

ANPC, SMC and RMC presents a balanced inner voltage, achieving five level output voltage. However, when the reference value is small, ANPC and SMC uses only three levels to generate the desired output voltage (inner vectors in Fig. 2.10 in chapter 2), but RMC needs to use the five levels to achieve the desired output voltage, this is due to the number of vectors able to balance the inner voltages.

The Total Harmonic Distortion (THD) for the output current and output voltage is shown in Table 5.3, and it is possible to see that there are not big differences between the RMC, ANPC and the SMC topology. As RMC uses five voltage levels in the case of low reference current, the THD of RMC in this case present a lower value than the THD for ANPC and SMC in the same case, but it is possible to see that this has not big impact in the THD of the current, for ANPC the current THD is 2.36 % and for RMC is 2.37 %.

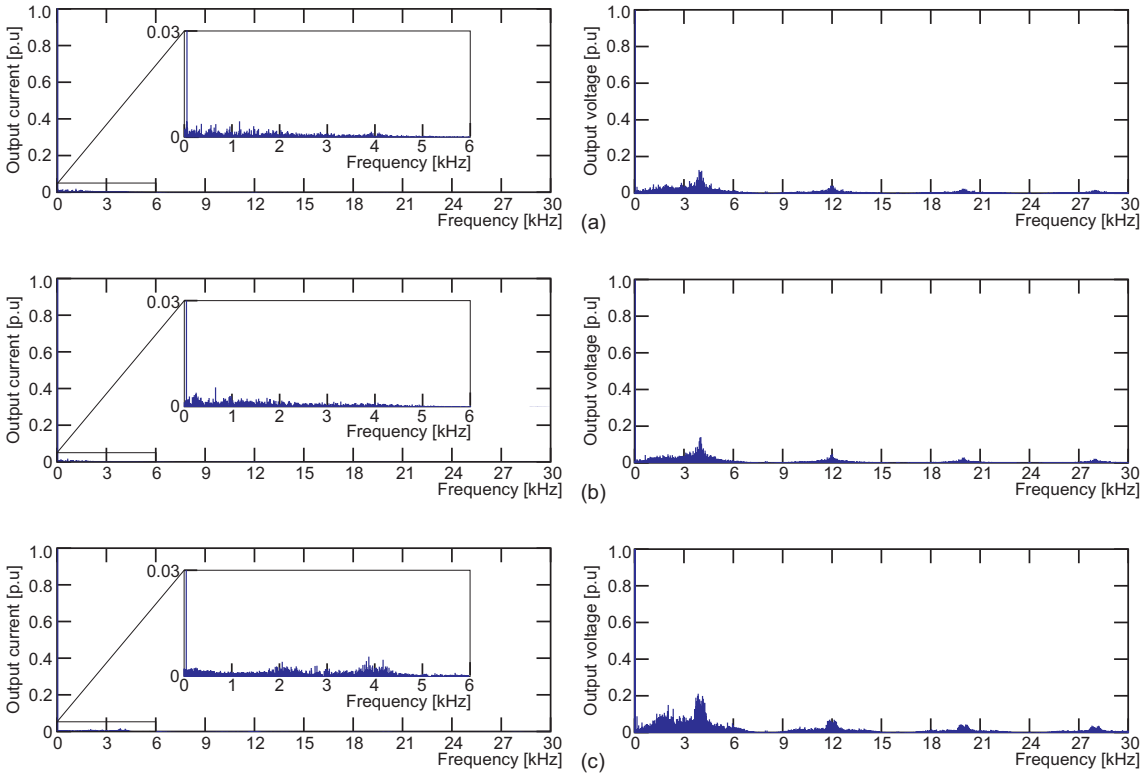


Figure 5.8. *Output currents and output voltage (v_{AN}) spectrum, for $\hat{i} = 15A$: (a) ANPC converter; (b) SMC converter; (c) RMC converter.*

Table 5.3
THD for 5-level topologies

Topology	Current THD		Voltage THD	
	15A	5A	15A	5A
ANPC	1.02 %	2.36 %	37.6 %	43.3 %
SMC	1.08 %	2.45 %	37.5 %	43.7 %
RMC	1.09 %	2.37 %	37.9 %	40.1 %

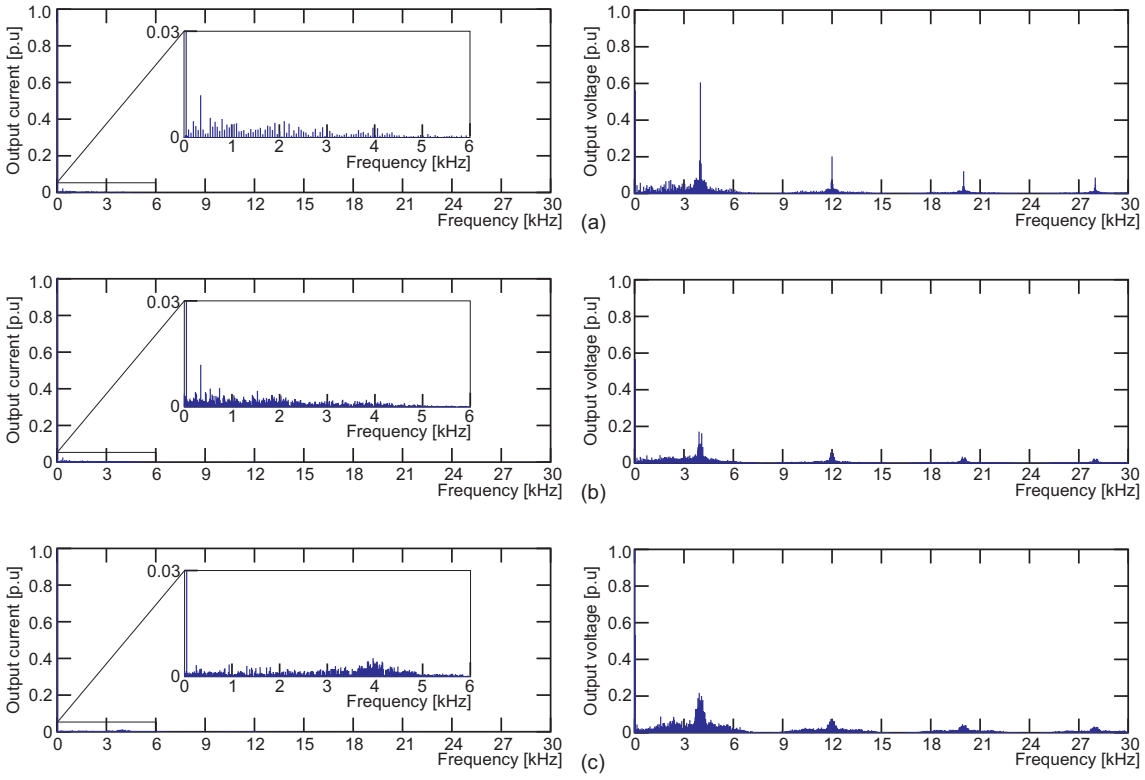


Figure 5.9. *Output currents and output voltage (v_{AN}) spectrum, for $\hat{i} = 5A$: (a) ANPC converter; (b) SMC converter; (c) RMC converter.*

Fig. 5.8 and Fig. 5.9 show the harmonic spectrum for the output current and output voltage in phase A. Comparable to the spectrum for the 3-level topologies, the output current spectrum is widely spread and changes significantly for the different operation points. In the output current spectrum of the RMC it is possible to see that the spectrum is concentrated around the 4kHz and ANPC and SMC current spectrum has a bigger harmonic in 350Hz.

In the output voltage spectrum, the harmonics are more concentrated than in the case of 3-level topologies around the 4kHz and its multiples, a clear effect of the increase of the number of output voltage levels of the converter. For ANPC topology, for low reference values, it is possible to see that there is a big harmonic around the switching frequency (4kHz).

Finally, to verify the dynamic behavior of the system, Fig. 5.10 shows the system response after a step in the current references, same step than in the case of 3-level topologies. The dynamic response in ANPC converter takes 1.99ms to achieve the new value, SMC takes 2.01ms and RMC converter 1.98ms. In addition, FCS-MPC achieves a balanced inner voltage even during the transient.

Consequently, RMC topology is scalable to 5 level with a comparable performance in steady-state and transient with other topologies, like ANPC and SMC.

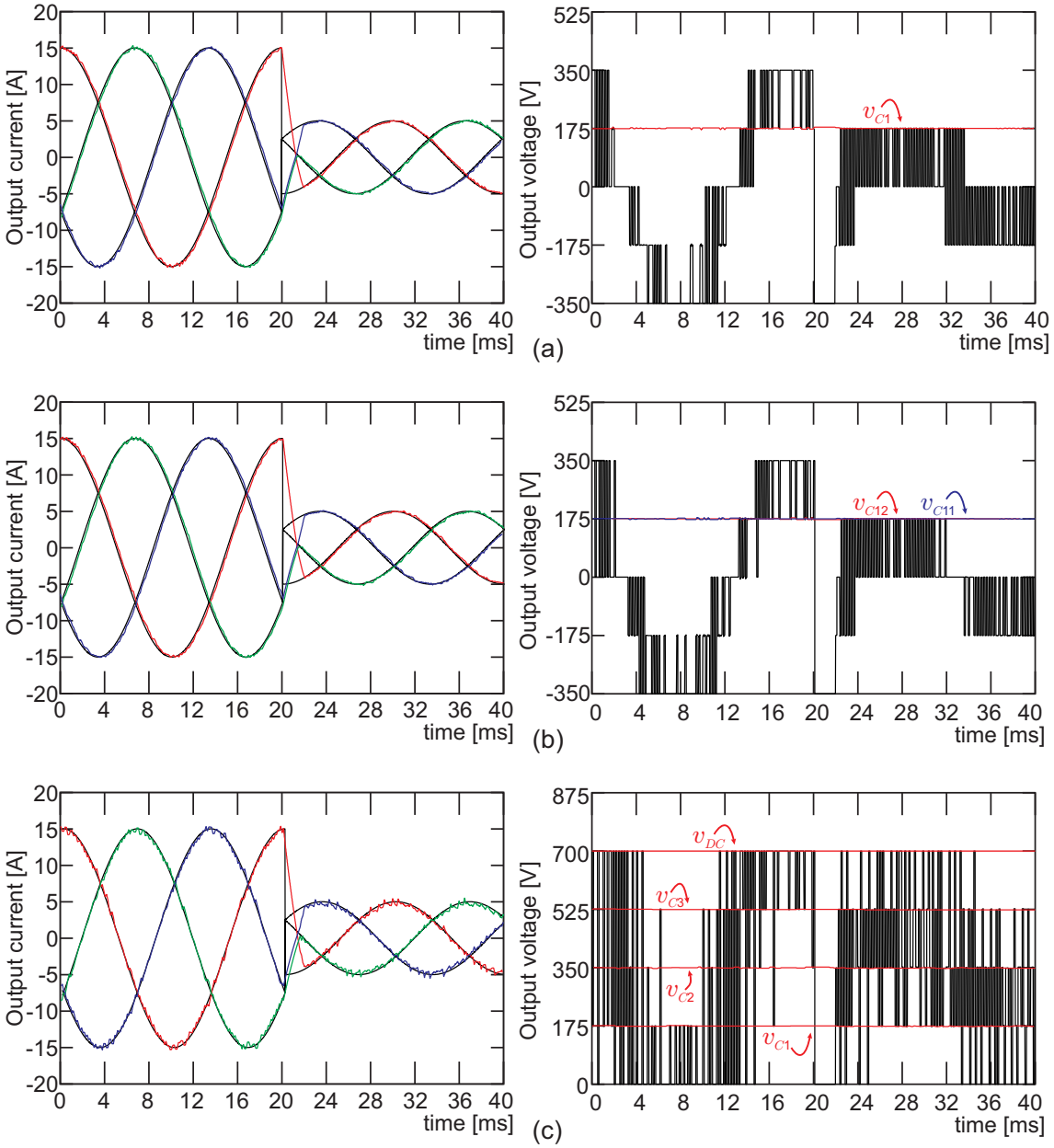


Figure 5.10. *Output currents and output voltage (v_{AN}). Dynamic response: (a) ANPC converter; (b) SMC converter; (c) RMC converter.*

5.2. Characteristics of the Structure

5.2.1. Blocking voltage

Table 5.4 shows the blocking voltage maximum and minimum for the different topologies simulated. In the case of RMC, the output switches need to block full *dc-link*. In T-type converter and SMC, the switches with maximum blocking voltage are the top and bottom ones (S_{1E2X}, S_{2E2X}, $\bar{S}_{1E1X}$, $\bar{S}_{2E1X}$). Finally, in the ANPC converter, the switches: S_{1A}, S_{2A}, S_{3A} and S_{4A}, are going to block half *dc-link* voltage.

Fig. 5.11 shows the blocking voltage in a 3L-RMC with $V_{DC} = 700V$. The 3L-RMC has one DC-cell, and the three power switches in this cell (S_{p1}, S_{n1} and S_{C1}) going to block half *dc-link* voltage as is shown in Fig. 5.11-(a). Nevertheless, the output switches (2L-VSI stage) going to block full *dc-link* voltage when $S_{p1} = 1$, $S_{n1} = 1$ and $S_{C1} = 0$, and going to block half *dc-link* voltage when $S_{p1} = 1$ (or $S_{p1} = 0$), $S_{n1} = 0$ (or, $S_{n1} = 1$) and $S_{C1} = 1$, as is shown in Fig. 5.11-(b).

Fig. 5.12 shows the blocking voltage in 5L-RMC for one period of the fundamental output voltage. The 5L-RMC has 3DC-cells in the DC-DC stage and the switches in the third DC-cell (S_{p3}, S_{n3} and S_{C3}) going to block a quarter of *dc-link* voltage as is shown in Fig. 5.12-(a). But power switches in second DC-cell (S_{p2}, S_{n2} and S_{C2}) some times going to block a quarter of *dc-link* voltage and some times half *dc-link* voltage. Power switches in the first DC-cell (S_{p1}, S_{n1} and S_{C1}) some times going to block three quarter of *dc-link* voltage, half *dc-link* voltage, or a quarter of *dc-link* voltage. Finally, the power switches in the output stage (2L-VSI) some times need to block full *dc-link* voltage, three quarter of *dc-link* voltage, half *dc-link* voltage, or a quarter of *dc-link* voltage as is shown in Fig. 5.12-(b).

Table 5.4
Blocking voltage for multilevel topologies

Topology	**Blocking Voltage**	
	maximum	minimum
NPC	$V_{DC}/2$	$V_{DC}/2$
T-type	V_{DC}	$V_{DC}/2$
RMC 3-level	V_{DC}	$V_{DC}/2$
ANPC	$V_{DC}/2$	$V_{DC}/4$
SMC	$V_{DC}/2$	$V_{DC}/4$
RMC 5-level	V_{DC}	$V_{DC}/4$

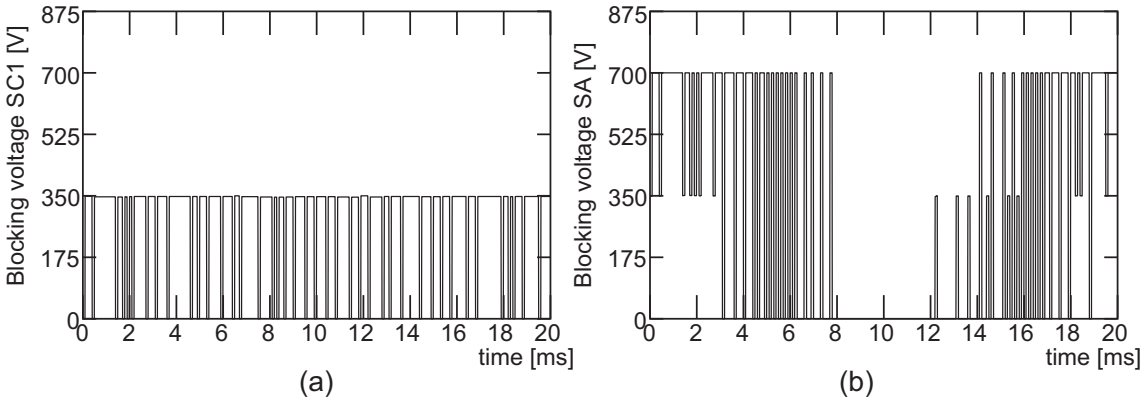


Figure 5.11. *Blocking voltage in 3-level RMC: (a) Switch S_{C1}; (b) Switch S_A.*

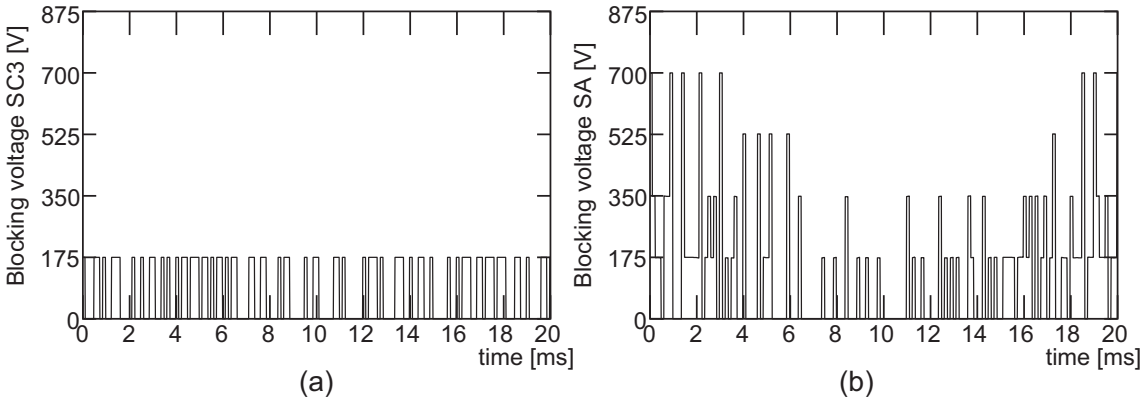


Figure 5.12. *Blocking voltage in 5-level RMC: (a) Switch S_{C3}; (b) Switch S_A.*

5.2.2. Switching frequency

Table 5.5 shows the average switching frequency for the different topologies simulated. To calculate the average switching frequency all commutations in one period of the fundamental signal are considered.

The switching frequency shown in Table 5.6 is calculated as follow:

$$\bar{F}_{sw} = \frac{1}{N}\sum_{i=1}^{N} \bar{F}_{sw}(S_i) \tag{5.5}$$

Where $\bar{F}_{sw}(S_i)$ is the average switching frequency for the generic power switch S_i, for example, in RMC there are $N = 15$ power switches and $S_i \in \{S_{pk}, S_{nk}, S_{Ck}, S_x, \bar{S}_x\}$, for $k \in \{1, 2, 3\}$ and $k \in \{A, B, C\}$.

In this work, FCS-MPC is used to control the system, and the cost function used is the given in the previous section, where it is controlled the output currents and the inner voltages of the converters. It was not included an additional term to ensure a fixed switching frequency because the focus of this study is to analyzed the topologies for a similar performance (similar system response with the same sampling frequency).

In the previous section (5.1) was shown that RMC has a comparable system response with other topologies, now an important point to review it is the necessary switching frequency to achieve those performances. However, as the control objective of FCS-MPC is not the switching frequency, this will change in function of the reference value of the current, the switching frequency will be higher for a low reference value when FCS-MPC is used, especially in 5L topologies because the control uses fewer voltage levels (3 instead 5) to generate the desired output voltage.

From the results shown in Table 5.5 it is possible to see that for high reference values, RMC topology has a comparable switching frequency with the other topologies, whatever, 3 level or 5 level topologies. Nevertheless, for a low reference value, RMC present a higher switching frequency in both cases, it is important to remember that in 5L-RMC, the converter uses five levels even for a low reference value, so the difference in the switching frequency in a 5L-RMC is due the converter and not the control strategy as is the case of the ANPC and SMC.

Nevertheless, RMC has an acceptable switching frequency in comparison with the other topologies, for low reference values the switching frequency is an acceptable value and for the five levels topology even is fewer than the switching frequency for ANPC.

Since RMC has a reduced number of possible switching states in comparison with other topologies, to ensure the tracking error in the control objectives, FCS-MPC decides an exotic commutation pattern and as consequence, the RMC has different switching frequency in its power switches as is shown in Table 5.6.

The switches S_{C3}, S_{C2} and S_{C1} are the switches in series connection with the flying capacitor in the DC-cells, and it is possible to see in Table 5.6 that these switches have a high switching frequency in comparison with other switches of the same DC-cell, which is congruent with the necessity of balance the inner voltages.

Table 5.5
Average switching frequency

Topology	**Switching frequency/Sampling frequency**	
	15A	5A
NPC	0.11	0.12
T-type	0.11	0.12
RMC 3-level	0.12	0.17
ANPC	0.12	0.21
SMC	0.11	0.16
RMC 5-level	0.11	0.18

Table 5.6
Switching frequency in 5-level RMC

Switch	Switching frequency	
	15A	5A
S_{p3}	1200Hz	1350Hz
S_{n3}	950Hz	1650Hz
S_{C3}	2050Hz	2100Hz
S_{p2}	850Hz	1600Hz
S_{n2}	800Hz	1700Hz
S_{C2}	1650Hz	1850Hz
S_{p1}	450Hz	1700Hz
S_{n1}	550Hz	1800Hz
S_{C1}	1000Hz	1900Hz
S_A	1300Hz	2000Hz

5.2.3. Switching and conduction losses

To determine the total power losses (switching and conduction) in the different converters, the thermal tools of PLECS® is used.

PLECS® has a domain for modeling thermal structures and calculating switching and conduction losses in switches by means of lookup tables based on manufacturer information or experimental measurements.

For a fair comparison, the simulation is carried out with the active devices according to the needs in every topology (this is blocking voltage and current rating). For more details about the losses calculation, please refer to appendix A.

Fig.5.13 show the total power losses for different output current values. It is possible to see that for 3-level topologies, the proposed converter has more power losses until $0{,}55I_{nom}$ output current, after this point, the proposed topology has fewer power losses. NPC and T-type converter have similar power losses for low output current and after $0{,}5I_{nom}$, 3L-RMC and NPC has comparable power losses.

Fig.5.13-(b) show the total power losses for 5-level topologies, the three topologies studied has almost the same power losses until $0{,}7I_{nom}$, after this operation point, 5L-RMC has fewer power losses and SMC has 30 % more power losses than ANPC and 5L-RMC.

Thus, the proposed topology has comparable power losses and depending on the output current, has better efficiency than other multilevel converts.

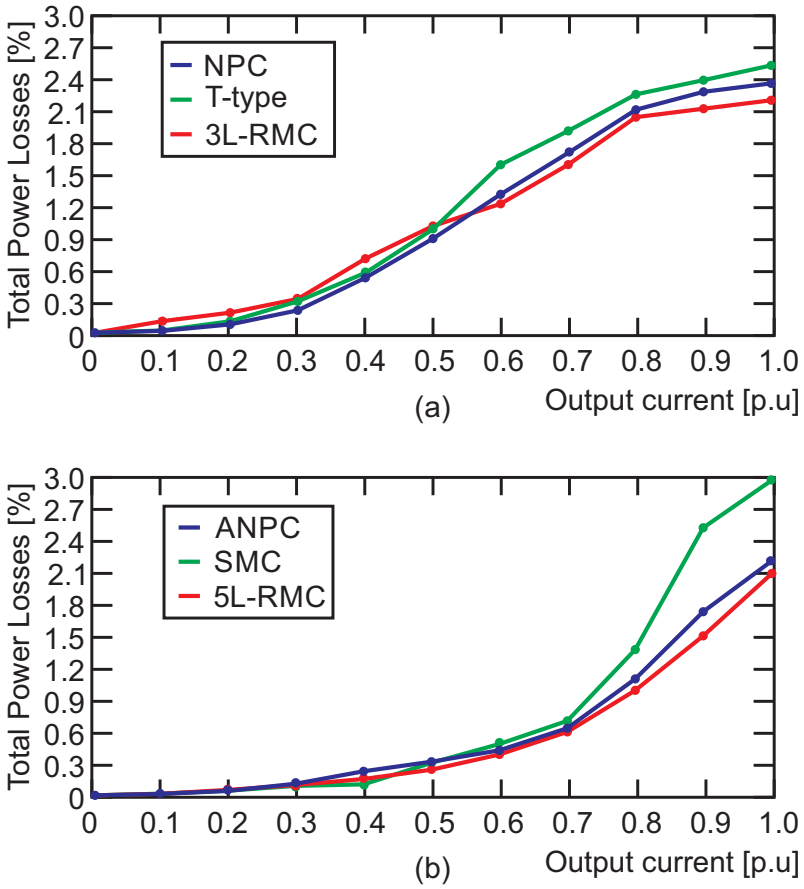


Figure 5.13. *Switching and conduction power losses for: (a) 3-level topologies, (b) 5-level topologies.*

5.2.4. Storage energy and size of the inner capacitors

The energy stored in the converter is given by:

$$\sum_{num.\,of\,capacitor} \frac{1}{2} C V^2 \tag{5.6}$$

With C the capacitance value and V the voltage across the capacitor.

The capacitance value is calculated to have a determinate ripple in the inner voltage. The capacitance is calculated using the equation (5.7).

$$C = \frac{1}{\Delta_v} \hat{i} T_s \tag{5.7}$$

Where T_s is the sampling period, $\hat{i}$ the maximum current through the capacitor and Δ_v the voltage variation in the capacitor.

For a maximum ripple of 5 % (Δ_v) in all inner capacitors, Table 5.7 shows the minimum capacitance in the different topologies to accomplish this task.

Table 5.7
Capacitance size

Topology	Capacitor	Capacitance [μF]	Capacitor Voltage
ANPC	C_{1X}	171.4	$V_{DC}/4$
SMC	C_{1E1}	171.4	$V_{DC}/4$
	C_{1E2}	171.4	$V_{DC}/4$
RMC	C_1	171.4	$V_{DC}/4$
	C_2	85.7	$V_{DC}/2$
	C_3	57.1	$3V_{DC}/4$

Table 5.8 shows the total energy stored in the different topologies simulated. The energy stored in the converter has direct relationship with the size of the inner capacitors. Thus the size of the inner capacitors in RMC are not bigger than the inner capacitors in SMC.

Table 5.8
Capacitance size

Topology	Energy stored [kWh]
NPC	0
T-type	0
RMC 3-level	2.92
ANPC	2.19
SMC	4.38
RMC 5-level	4.38

5.3. Comments

RMC topology has similar behavior and structure characteristic than the standard and commercial topologies like NPC, ANPC and SMC.

However, RMC has less active components than these topologies, Fig. 5.14 shows the different topologies for three level and Fig. 5.15 shows the different topologies for five level.

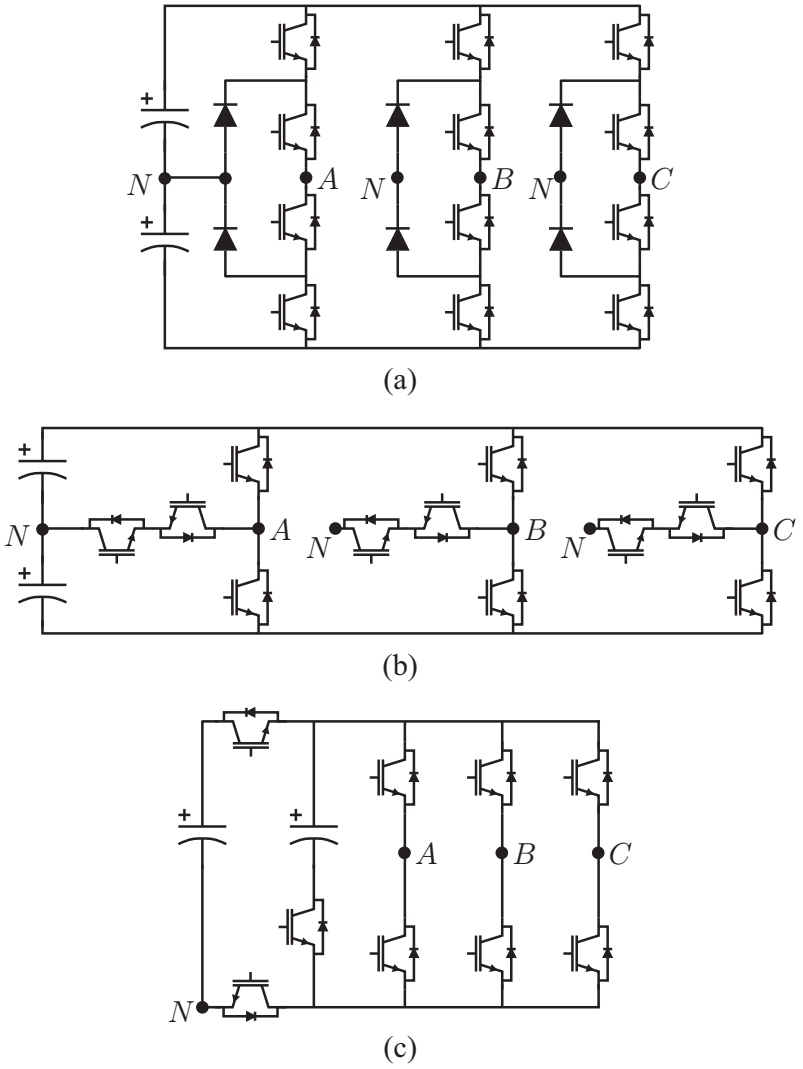


Figure 5.14. *Three level converters: (a) NPC; (b) T-type; (c) 3L-RMC.*

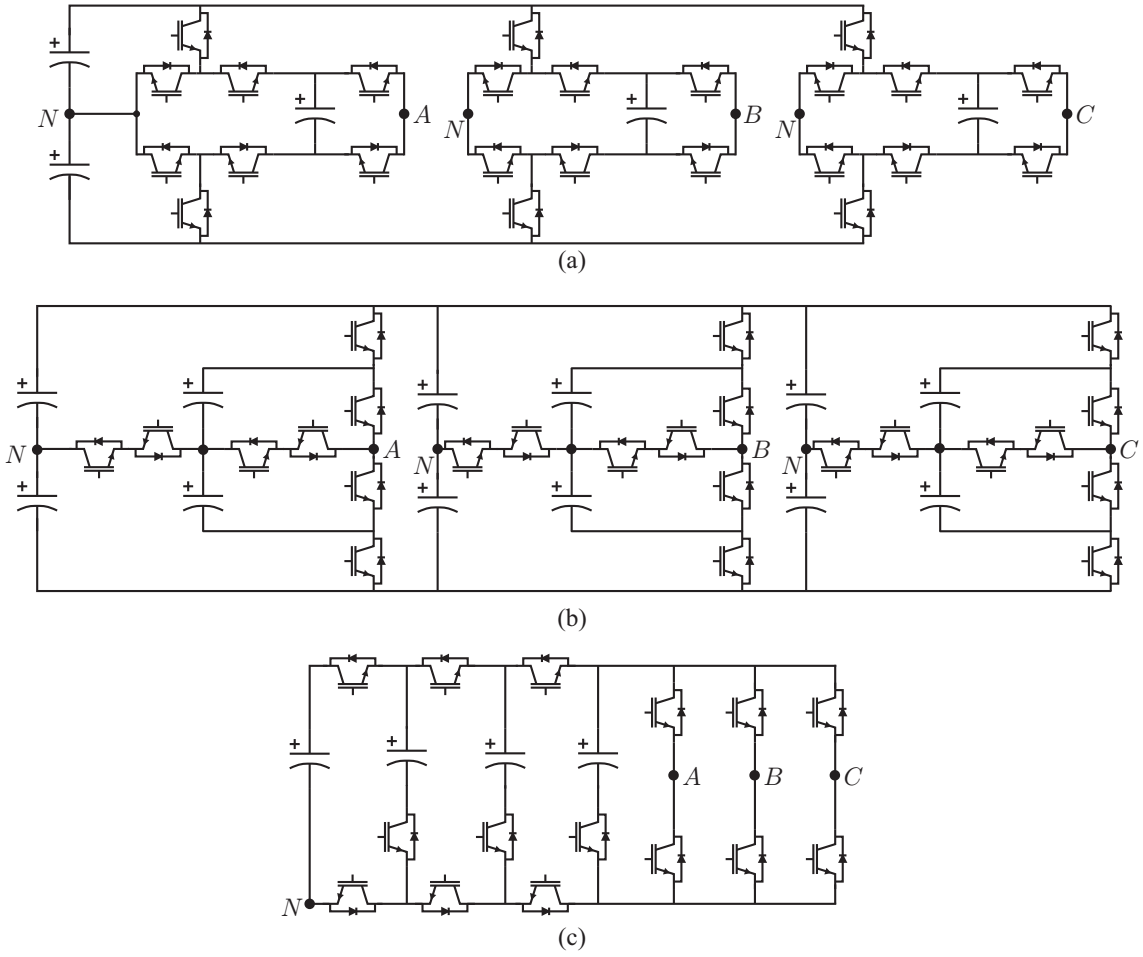


Figure 5.15. *Five level converters: (a) ANPC; (b) SMC; (c) 5L-RMC.*

5.4. Back-to-Back RMC

An interesting configuration that RMC can achieve easily is the back to back, which consists of the connection of two converters, one as AC-DC rectifier from the grid and another as DC-AC inverter to the load, sharing the same *dc-link* capacitor.

For RMC, the back to back connection only means six additional output switches for the three additional output phases. To show how RMC works in this case, a back to back connection is simulated between the grid and an Induction Machine (IM) as is shown in Fig. 5.16.

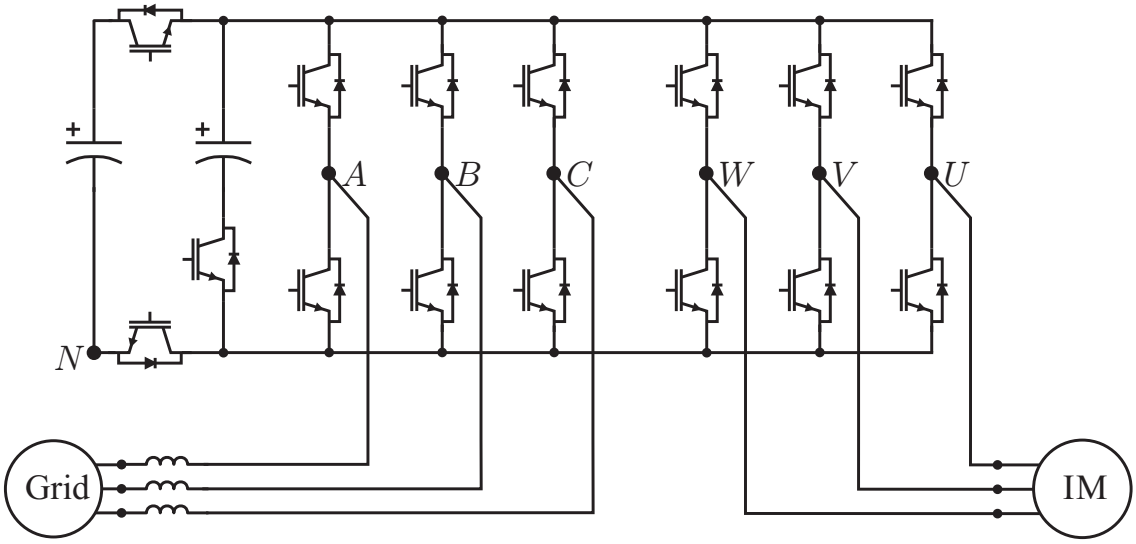


Figure 5.16. *3L-RMC back to back connection.*

The control in the machine is a Torque-Flux control without speed loop and has a mechanical load of $T_{load} = T_{nom}$, and the control in the grid is a power control. The cost function for FCS-MPC is:

$$g^{k+1} = \left(i_A^* - i_A^{k+1}\right)^2 + \left(i_B^* - i_B^{k+1}\right)^2 + \left(i_C^* - i_C^{k+1}\right)^2 + \lambda_1 \left(v_{C1}^* - v_{C1}^{k+1}\right)^2 + \left(T^* - T^{k+1}\right)^2 + \lambda_2 \left(\psi^* - \psi^{k+1}\right)^2 \tag{5.8}$$

Where $\lambda_1 = I_{nom}/v_{C1_{nom}}$ and $\lambda_2 = T_{nom}/\Psi_{nom}$. The control strategy needs to evaluate 192 possible switching states. To control the *dc-link* voltage is used a linear controller (PI):

$$C = 0{,}3397\frac{(z - 0{,}93)}{(z - 1)} \tag{5.9}$$

The most relevant parameters of the machine and control are detailed in Table 5.9.

Table 5.9
Simulation parameters for back to back connection

Parameter	Value
Voltage *dc-link*	700 V
Inductance grid filter	15 mH
Inner Capacitor	300 μF
DC-link Capacitor	600 μF
T_{nom}	50 N
P_{nom}	2.5 kW
Ψ_{nom}	0.71 Wb
L_m	170 mH
L_s	175 mH
L_r	175 mH
R_s	1.2 ω
R_r	1.0 ω
J	0.062 kgm^2
Sampling period	200 μs

The response of the system when a step in the Torque reference from $T^* = T_{nom}$ to $T^* = -T_{nom}$ is made, is shown in Fig. 5.17 and in Fig. 5.18. In this case, it is set a unitary power factor on the grid side, however, it is possible to set a different power factor. The active power reference for the grid is getting from the control over the *dc-link* voltage and the reactive power reference is given from the user.

It is possible to see in Fig. 5.17-(a) that the control strategy achieves a sinusoidal input current with unitary power factor (PF=1) in the steady-state. Additionally, the *dc-link* and inner capacitor voltage are controlled in the desired value with an acceptable minimum ripple, Fig. 5.17-(b). The *dc-link* voltage presents a perturbation only when the Torque step is made, because the machine is in regenerative zone and the *dc-link* controller has a low dynamic response. Finally, the output currents in the machine side, Fig. 5.17-(c) are sinusoidal without perturbations or low-frequency harmonics.

Fig. 5.18 shows the mechanical response of the system. It is possible to see that the FCS-MPC presents a zero-error in the torque and flux during the steady-state and achieves a fast response after the step in the torque reference value. The speed of the machine is not controlled, thus the results shown in Fig. 5.18-(c) is only a consequence of the torque and flux control of the machine.

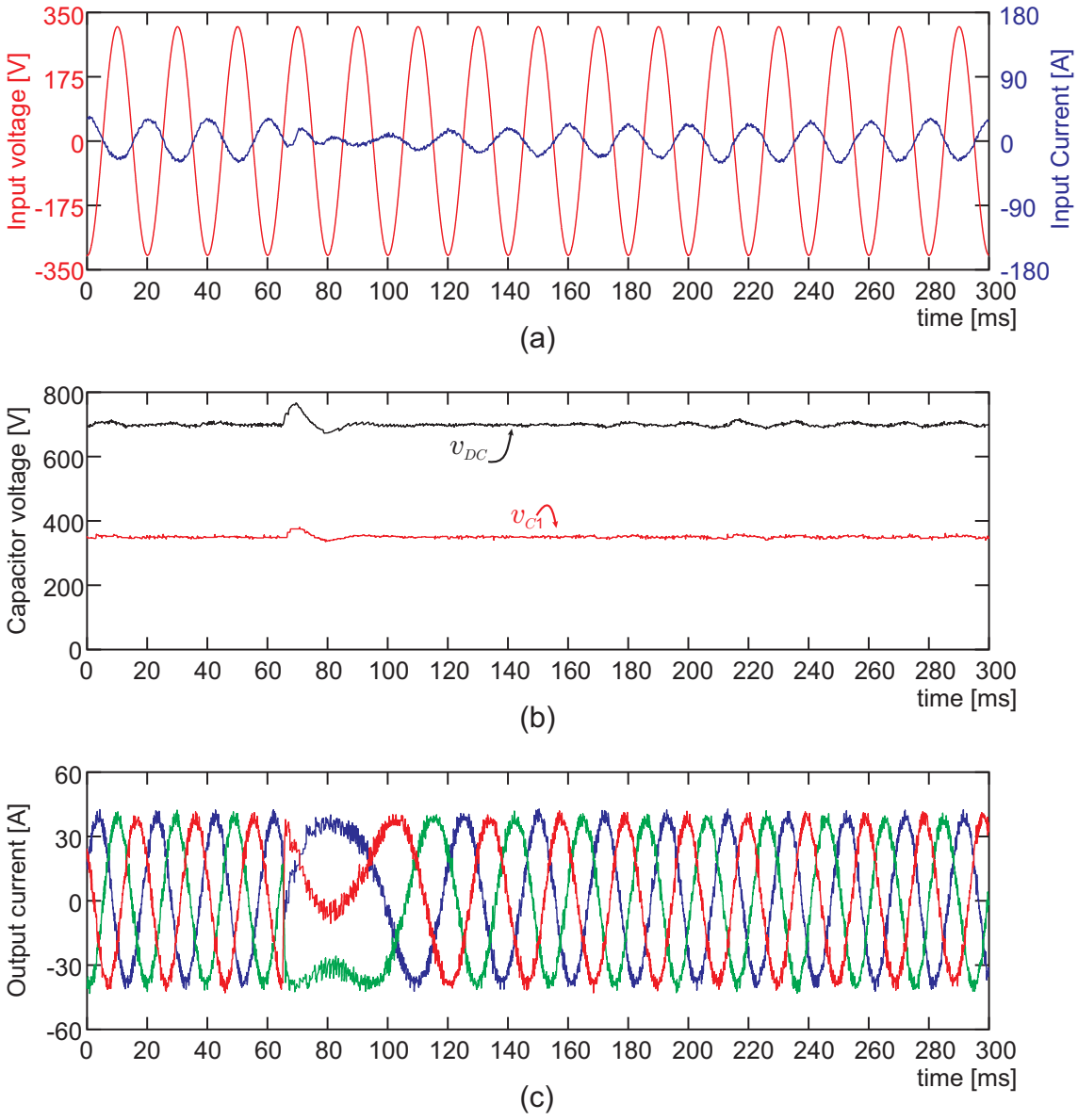


Figure 5.17. *3-level RMC back to back with a Torque step: (a) Grid side, voltage and current; (b)* DC-link *and inner capacitor voltages; (c) Machine output current.*

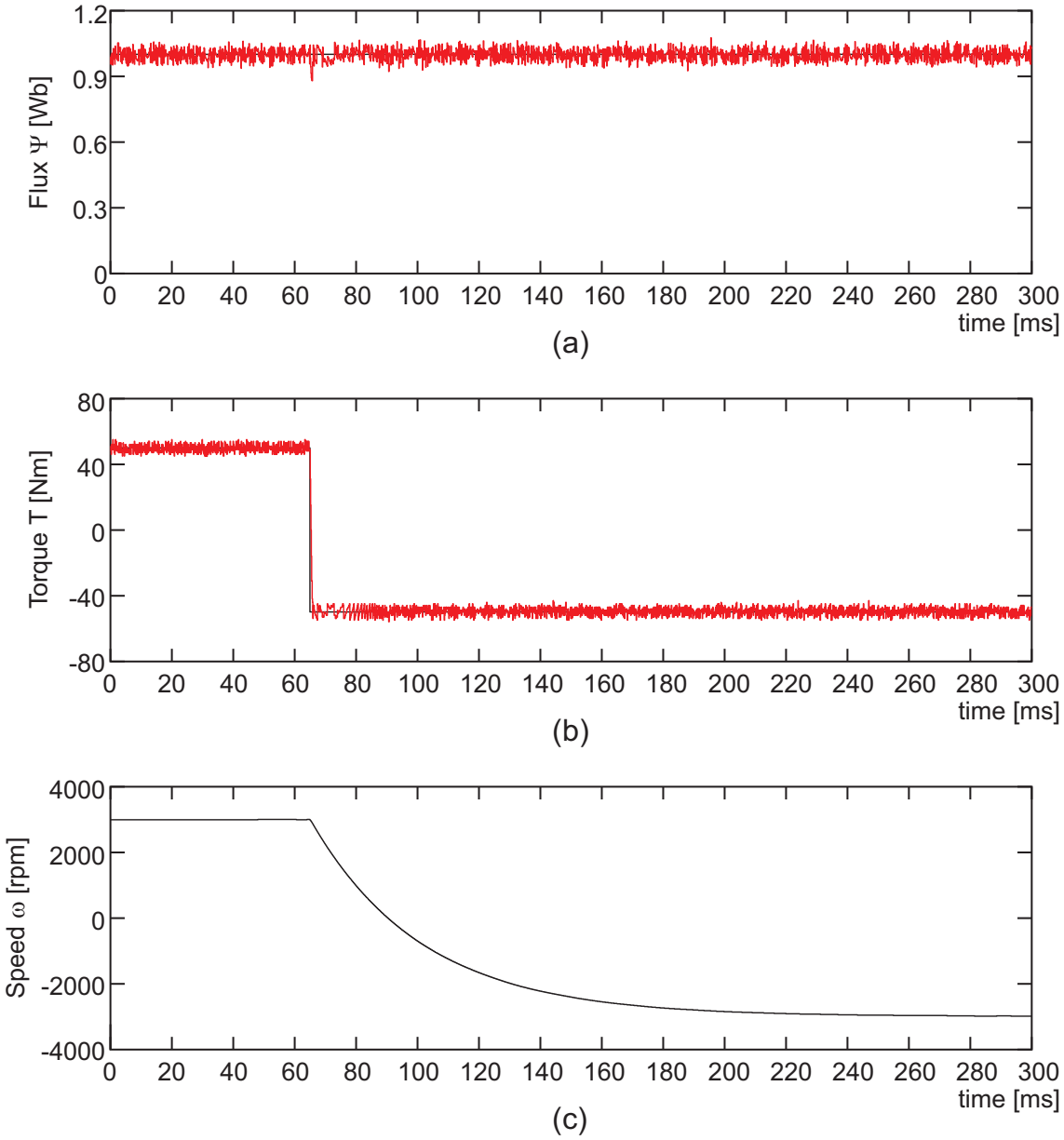


Figure 5.18. *3-level RMC back to back a Torque step: (a) Flux; (b) Torque; (c) Speed.*

Fig. 5.17 and Fig. 5.18 show that the back-to-back 3L-RMC works fine when a step in the machine side control is made, now it is presented the response of the system when a step in the Reactive Power reference, from $Q^* = 0$ to $Q^* = -0{,}3P_{nom}$, is made.

These results are shown in Fig. 5.19 and Fig. 5.20. In this case the PF changes from $PF = 0$ to $PF = 0{,}92$ capacitive.

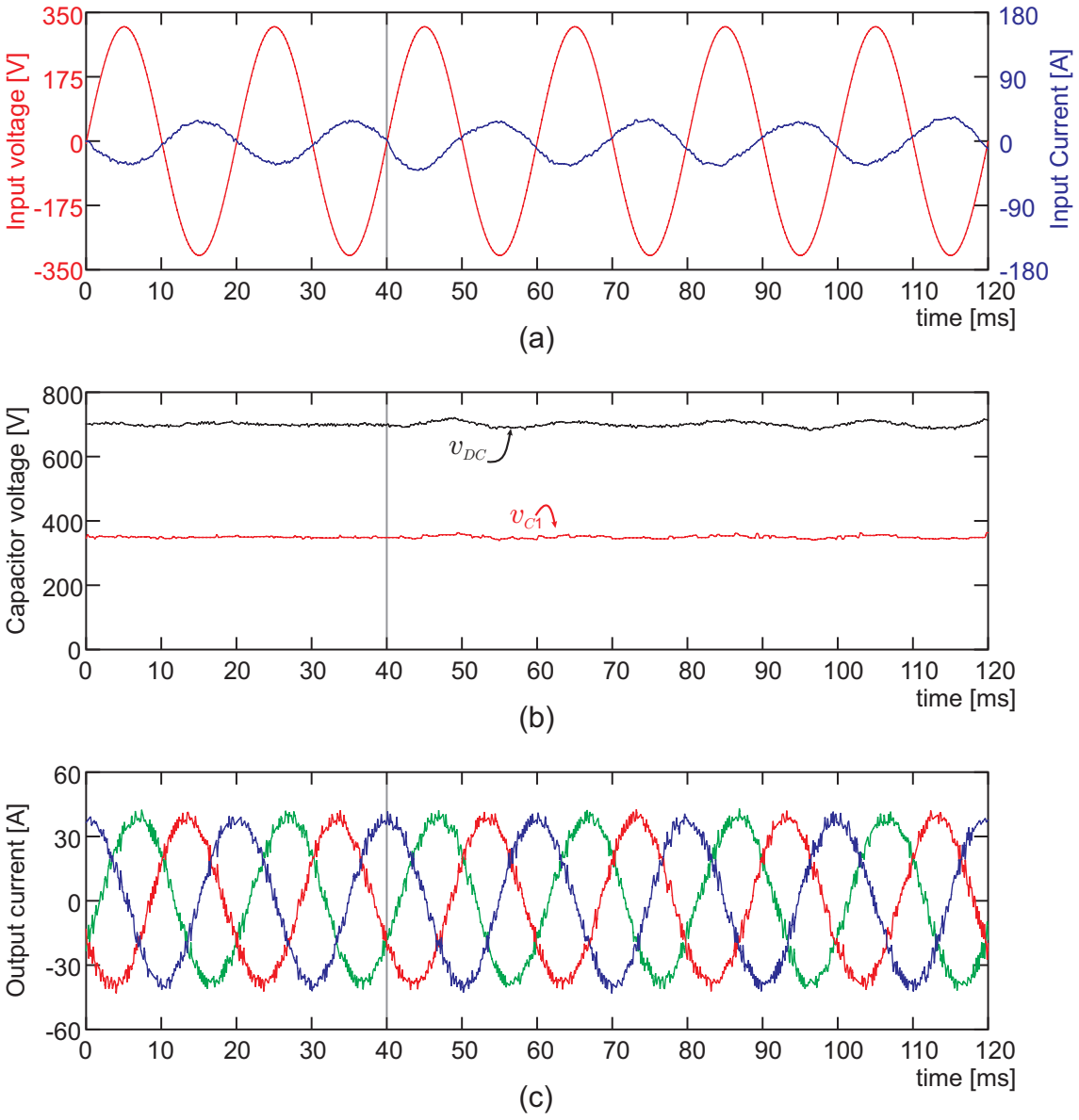


Figure 5.19. *3-level RMC back to back a Power step: (a) Grid side, voltage and current; (b)* DC-link *and inner capacitor voltages; (c) Machine output current.*

Fig. 5.19 shows the electric variable of the system when the power step is made at 40ms. It is possible to see that the step in the grid power has not influence in the machine current, Fig. 5.19-(c). However, after the power step, the *dc-link* voltage presents an oscillation of 1.4 %, Fig. 5.19-(b), it is a small oscillation, is not significant, and does not have influence in the inner voltage, where not appreciable oscillation is presented. Finally, in Fig. 5.19-(a) it is possible to see the sinusoidal output current with the different phase after the power step.

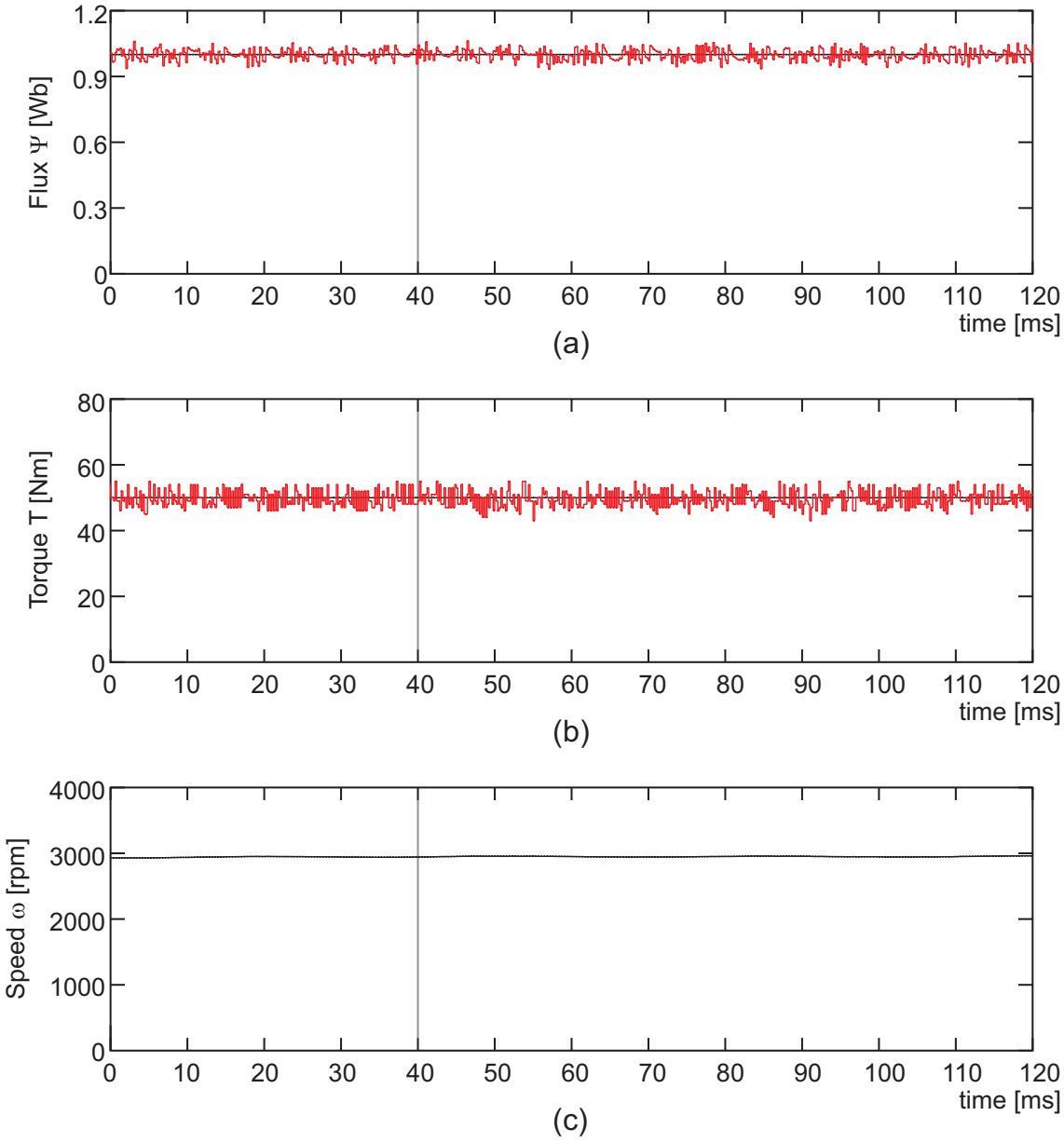


Figure 5.20. *3-level RMC back to back a Power step: (a) Flux; (b) Torque; (c) Speed.*

Like the machine current presented in Fig. 5.19-(c), the mechanical variables shown in Fig. 5.20 has not difference in their steady-state performance after the power step in the grid side. FCS-MPC controls the torque and flux with zero-error in steady-state and there is not appreciable perturbing due the power step.

Chapter 6

Experimental Validation

To evaluate the performance of the proposed topology, several experiments were carried out in the laboratory. The proposed topology was evaluated in both, dynamic and stationary state for a current reference of 50Hz. The controller was implemented on a Dspace MicroLabBox where the maximum time required by the control platform to execute the control code is 56,4μs. The most relevant parameters of the test-bench and controller are detailed in Table 6.1. For more details about the test bench, please refer to appendix B.

Table 6.1
Test bench parameters.

Parameter	Value
Voltage *dc-link*	400 V
Load Resistance	16 Ω
Load Inductance	30 mH
Inner Capacitors	330 μF
Sampling period	100 μs

6.1. Steady State Behavior

The purpose of this test is to assess the performance of the system once steady state has been reached for output current references of 75,8 %I_{nom} and 37,9 %I_{nom}.

The frequency spectrum of the current in phase A and the output voltage v_{AN}, the total harmonic distortion of these variables and ripple in inner capacitor voltages shall be analyzed.

Fig. 6.1 and Fig. 6.2 show the steady state performance of the converter with different output current references. The FCS-MPC algorithm can perform properly all control tasks, achieving sinusoidal three-phase output current and ensuring balanced inner voltages. The control results in five output levels in all phases.

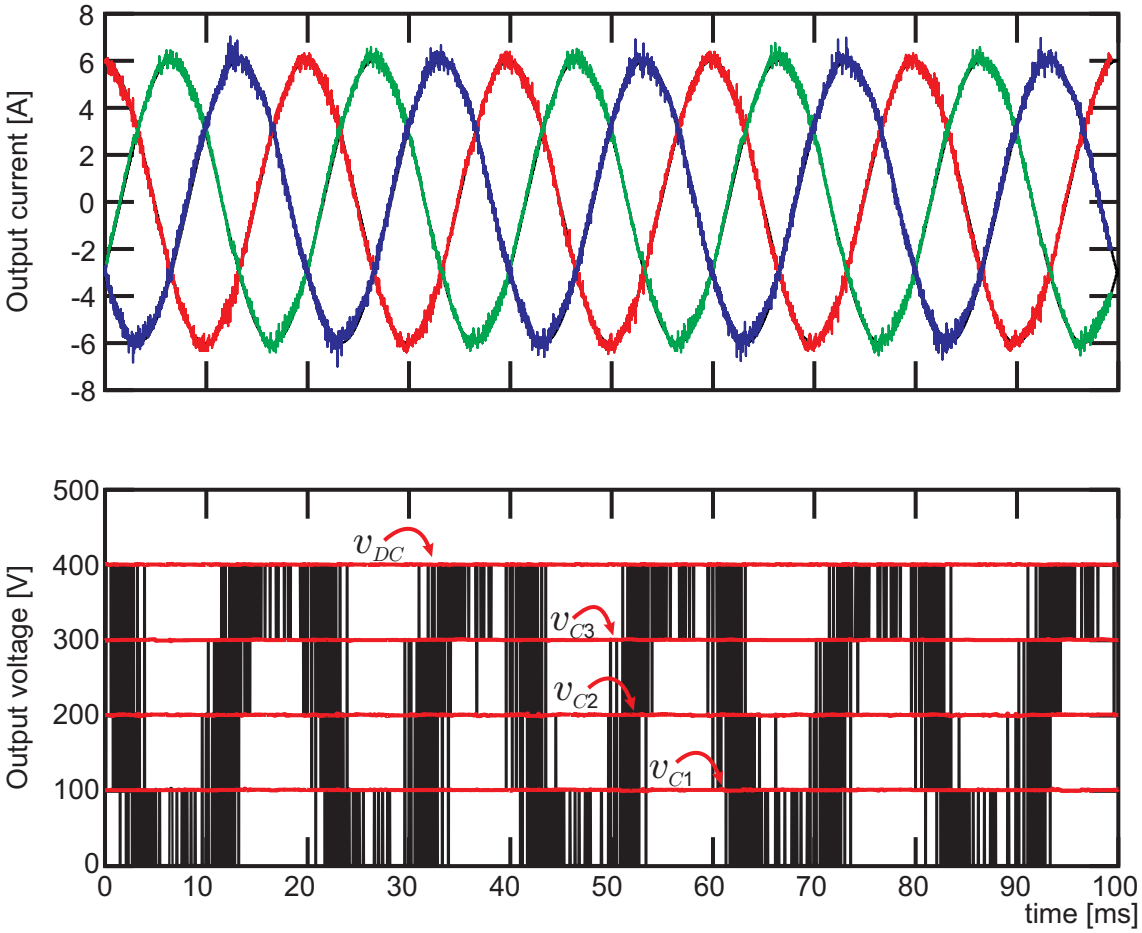


Figure 6.1. *Output current, output voltage v_{AN} and capacitor voltage with $i^* = 6sin(\omega t)A$.*

It is possible to see in the experimental results shown in Fig. 6.1 and Fig. 6.2 that 5L-RMC generate an output voltage (V_{AN}) with five levels in both low or high reference current.

For low reference current, Fig. 6.2, it is possible to see a higher ripple in the current 1,4 % of the reference current, but for high reference current this ripple is 0,8 % of the reference current. The change in the size of the current ripple is a consequence of the control strategy, FCS-MPC has the width of the switching signals limited to the sampling period, i.e a finite possibility instead of a variable width as in PWM modulations, and as consequence, for low reference value, FCS-MPC has a higher ripple. Nevertheless, in the case of the RMC, this effect is also a consequence of the lesser number of possible switching state in the converter, because to achieve the desired inner voltage, the RMC going to commutate between higher output voltages (uses the five levels).

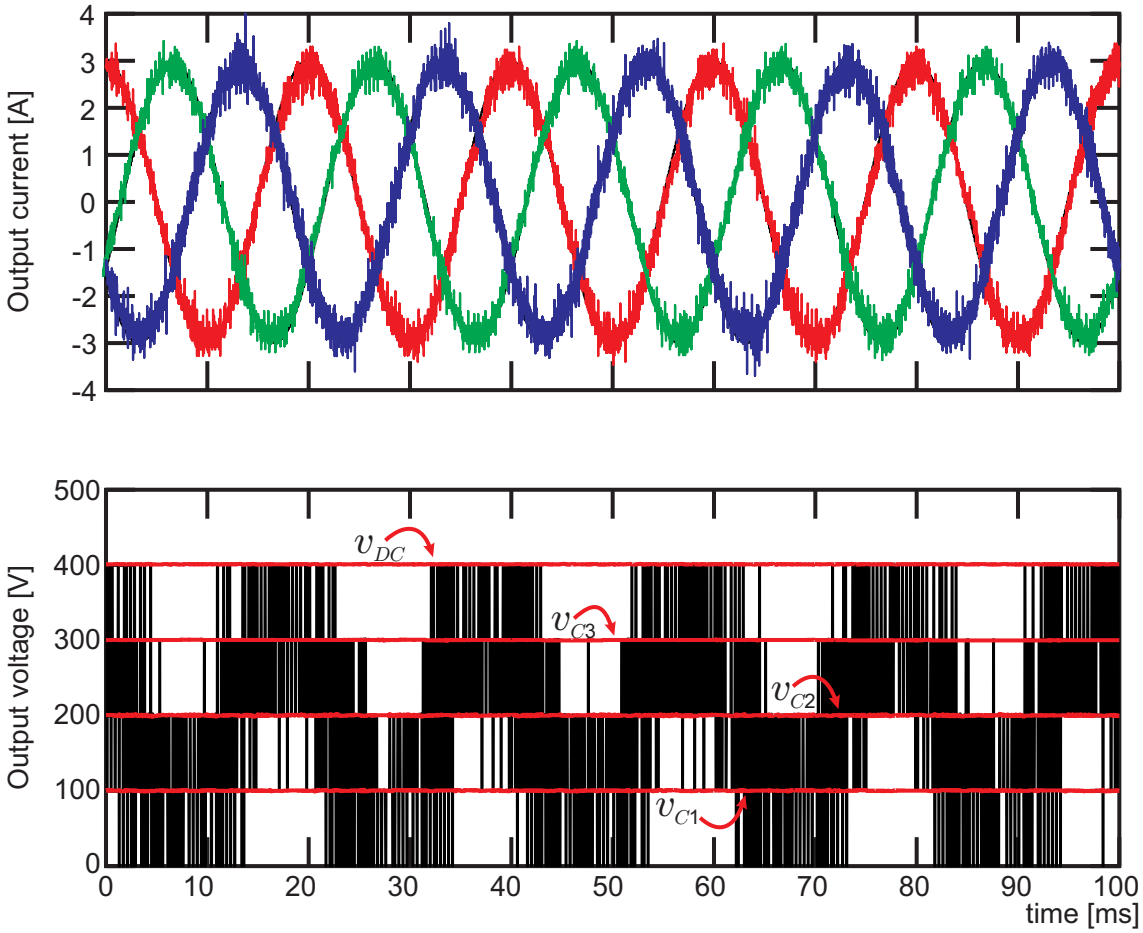


Figure 6.2. *Output current, output voltage v_{AN} and capacitor voltage with $i^* = 3sin(\omega t)A$.*

Fig. 6.3 and Fig. 6.4 show the inner capacitor voltages of the converter. The maximum ripple considering the capacitance of the flying capacitors are: 2,27 % for C_1, 1,14 % for C_2 and 0,76 % for C_3 with $\hat{i} = 6A$ and 1,13 % for C_1, 0,57 % for C_2 and 0,38 % for C_3 with $\hat{i} = 3A$. However, FCS-MPC strategy, through the weighting factors, ensures an equal maximum voltage ripple for the three capacitor voltages independent of the output current.

In the case of low output current, Fig. 6.2, FCS-MPC chooses output vectors with a greater influence on the inner capacitors voltages, specifically in C_1 and C_2, because it is necessary to commutate more often between 100V, 200V, and 300V to comply with the output current requirements.

The 5L-RMC produces an output voltage with 45.5 % total harmonic distortion (THD) for high reference values, whereas for low reference values with 50.8 %. Fig. 6.5 and Fig. 6.6 show the output current i_A spectrum and output voltage V_{AN} spectrum for both operation points.

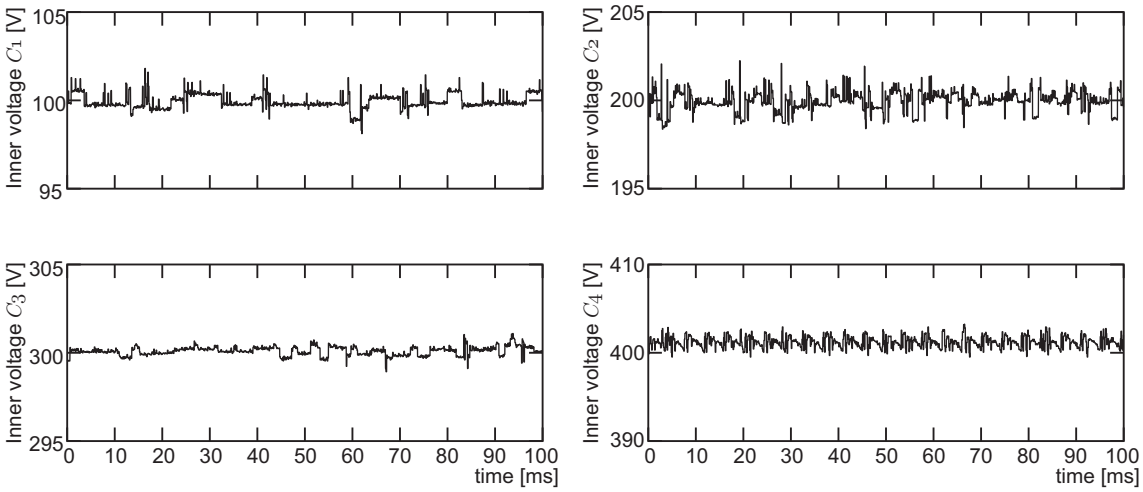


Figure 6.3. *Inner capacitor voltages for* $i^* = 6sin(\omega t)A$.

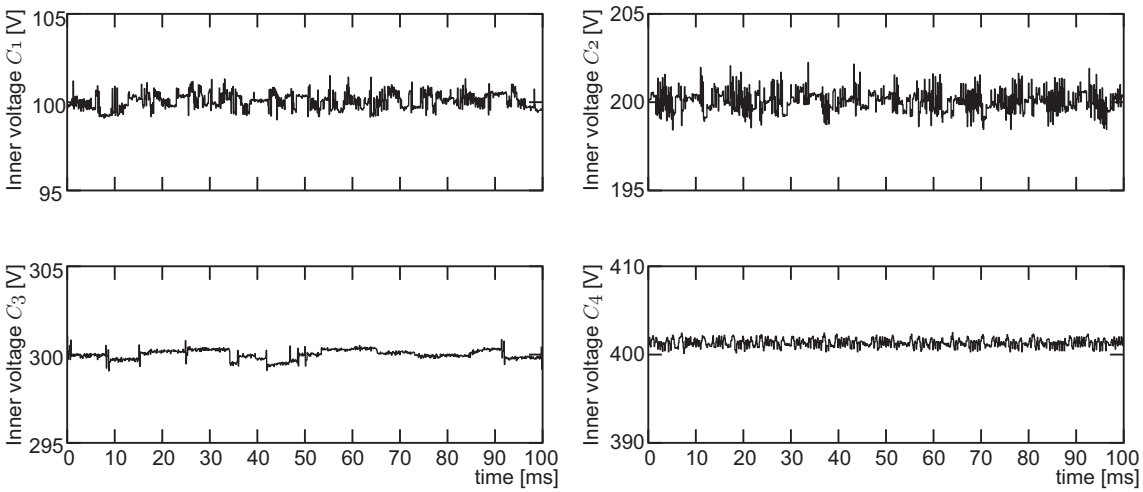


Figure 6.4. *Inner capacitor voltages for* $i^* = 3sin(\omega t)A$.

The sampling frequency of the FCS-MPC strategy is 10kHz, but the mean switching frequency is 5kHz. The Total Harmonic Distortion (THD) for the output current is: 4,45 % for $\hat{i}_A = 6A$ and 8,41 % for $\hat{i}_A = 3A$. It is possible to see that the THD increase and the spectrum changes significantly with the value of the reference.

The output current spectrum and output voltage spectrum shown in Fig. 6.5 and Fig. 6.6 is widely spread, but in the case of output voltage has a high concentration around the switching frequency (5kHz), which is more clear in Fig. 6.6, where even the output current spectrum presents a higher concentration around the 5kHz. However, it is possible to see that the output current spectrum presents an important number of low-frequency harmonics with a significative value (higher than the harmonic around 5kHz), these harmonic can produce resonant problems in the system and as they are widely spread, is not easy to filter them.

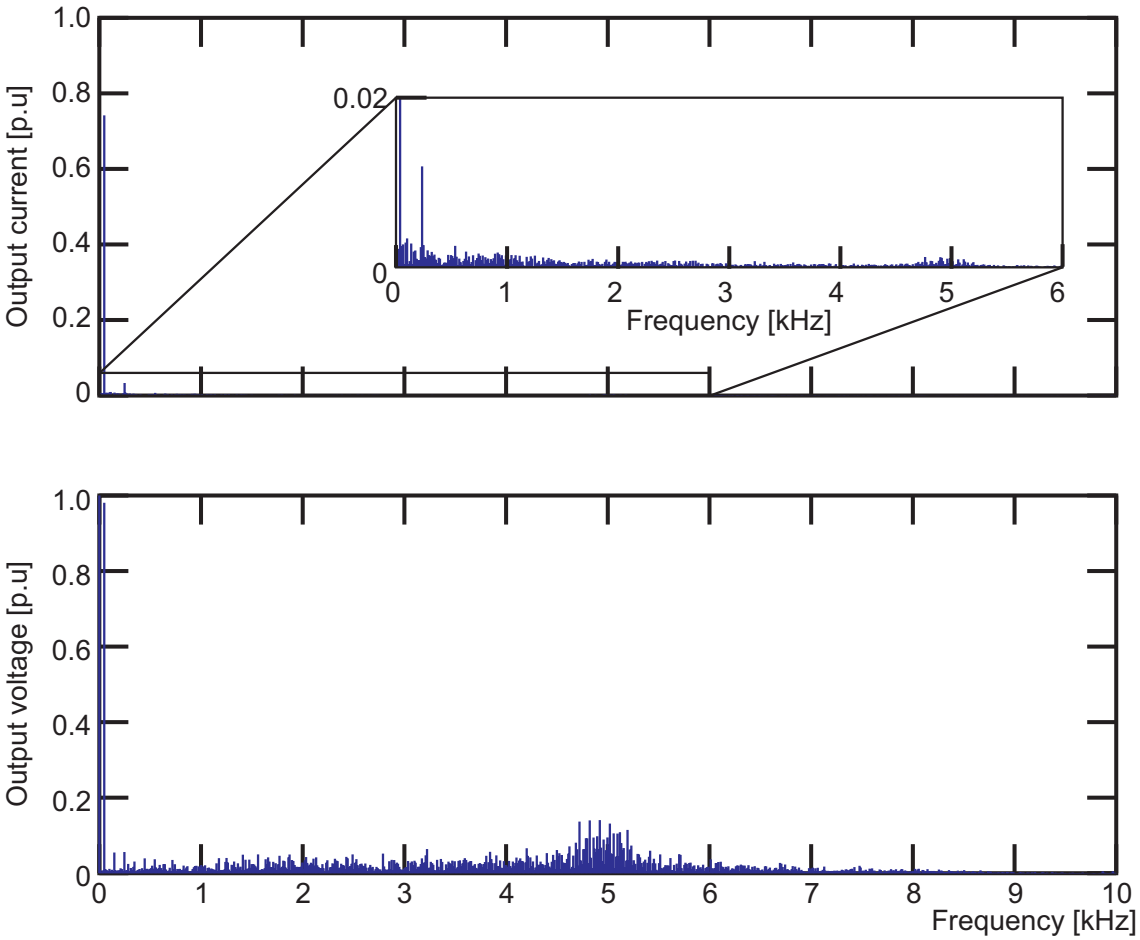


Figure 6.5. *Output current and output voltage v_{AN} harmonic spectrum for $i^* = 6sin(\omega t)A$.*

Finally, Fig. 6.7 shows the output current in phase A and the blocking voltage in the power switch S_9, this is the power switch in series with the capacitor in the main cell 1. In one period of the main variable, the switch S_{C1} needs to block different voltage levels. In Fig. 6.7 the different levels of the inner capacitors are indicated as a reference. As was shown in chapter 3, section 3.2.1, Table 3.6, switch S_{C1} sometimes needs to block $3V_{DC}/4$.

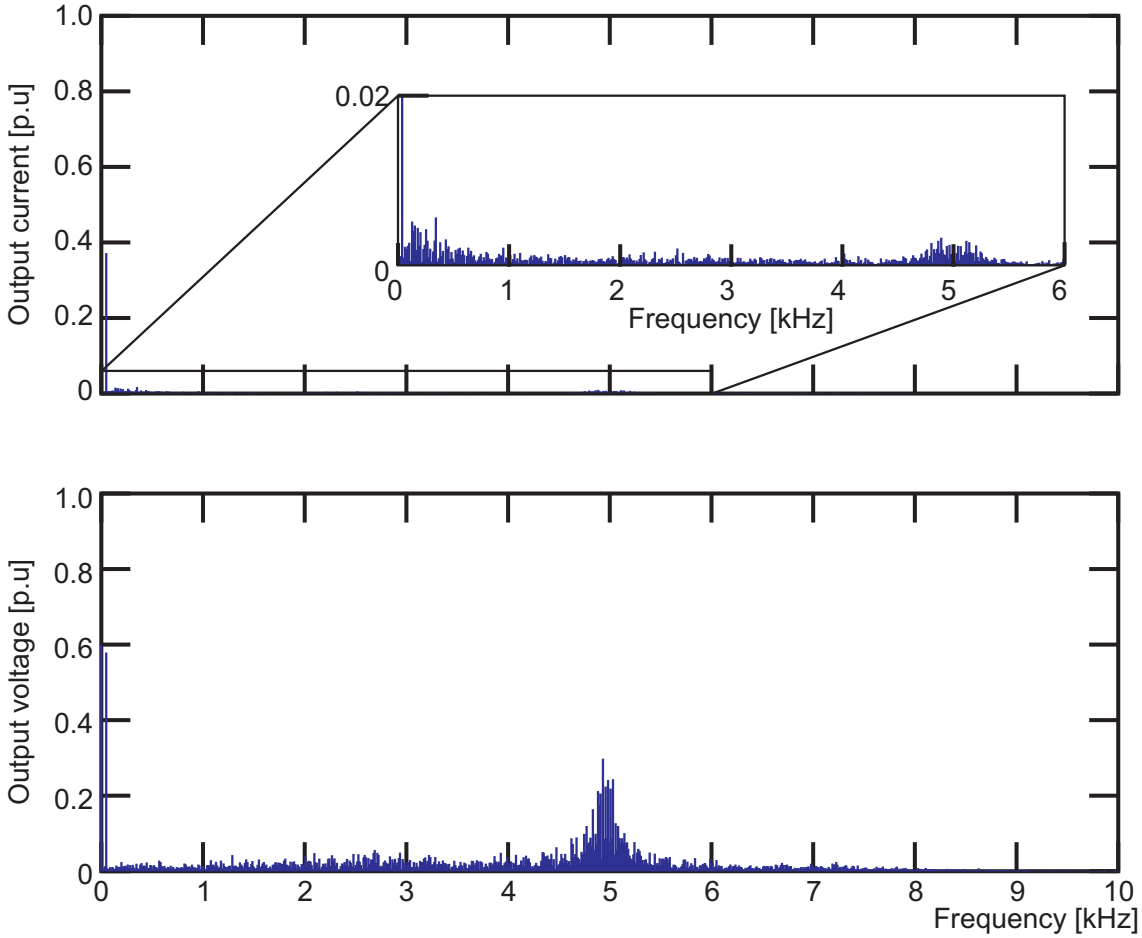


Figure 6.6. *Output current and output voltage v_{AN} harmonic spectrum for $i^* = 3sin(\omega t)A$.*

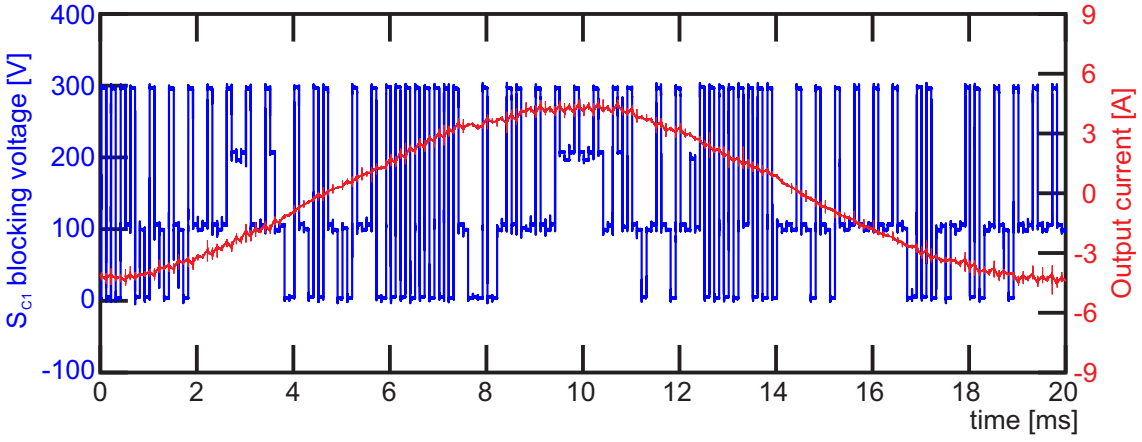


Figure 6.7. *Output current and blocking voltage in power switch S_{C1}.*

6.2. Dynamic Response

The purpose of this test is to demonstrate the behavior of the system in the presence of a variation in current reference values, bringing the system to a new steady-state working point.

It has been established for this test a quite demanding step. This is done with the purpose of verifying that the implemented control is able to achieve a performance according to the specifications required, regardless of the disturbances to which it is exposed. Therefore, the step performed not only changes the reference signal's magnitude, but also performs a phase change corresponding to a displacement at 180°.

Fig. 6.8 shows a zoom of the inner capacitor voltages during the step. In a more detailed picture, it is possible to check the fast response of FCS-MPC and the null disturbance in the inner capacitors voltages during the dynamic step. Voltage in capacitor C_4 represents the voltage in the DC power supply, in this case, the extra energy generated during the dynamic step results in a disturbance in the dc-link voltage.

Fig. 6.9 shows the performance of the converter in a dynamic step in the current reference. The control strategy ensures a correctly balanced voltage in the flying capacitors and a sinusoidal output current even during the transient time. In this case, FCS-MPC achieves a fast response of the variables, ensuring always a well balanced inner voltage and achieve the new steady-state operation point takes only 2.2ms (11 % of the fundamental period).

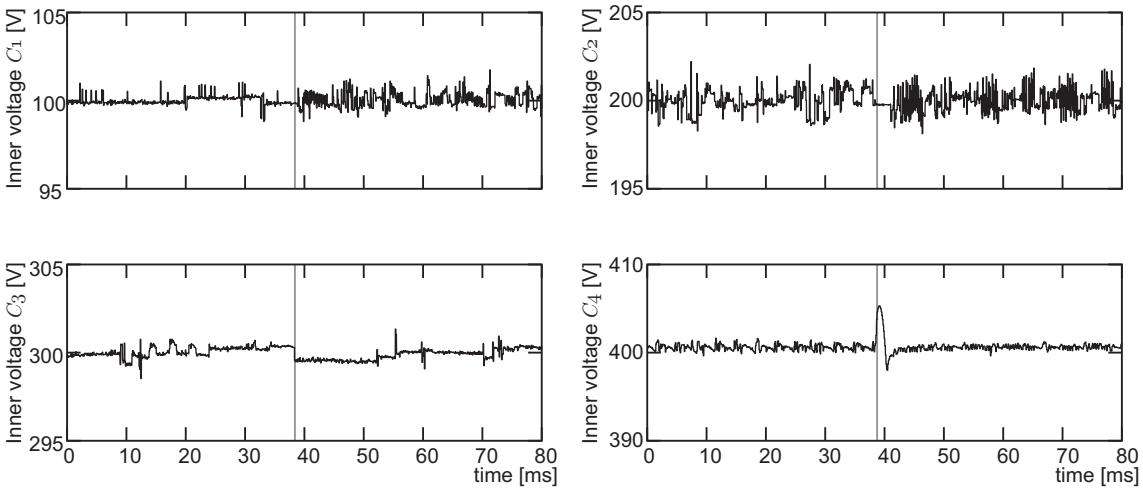


Figure 6.8. *Inner capacitor voltages.*

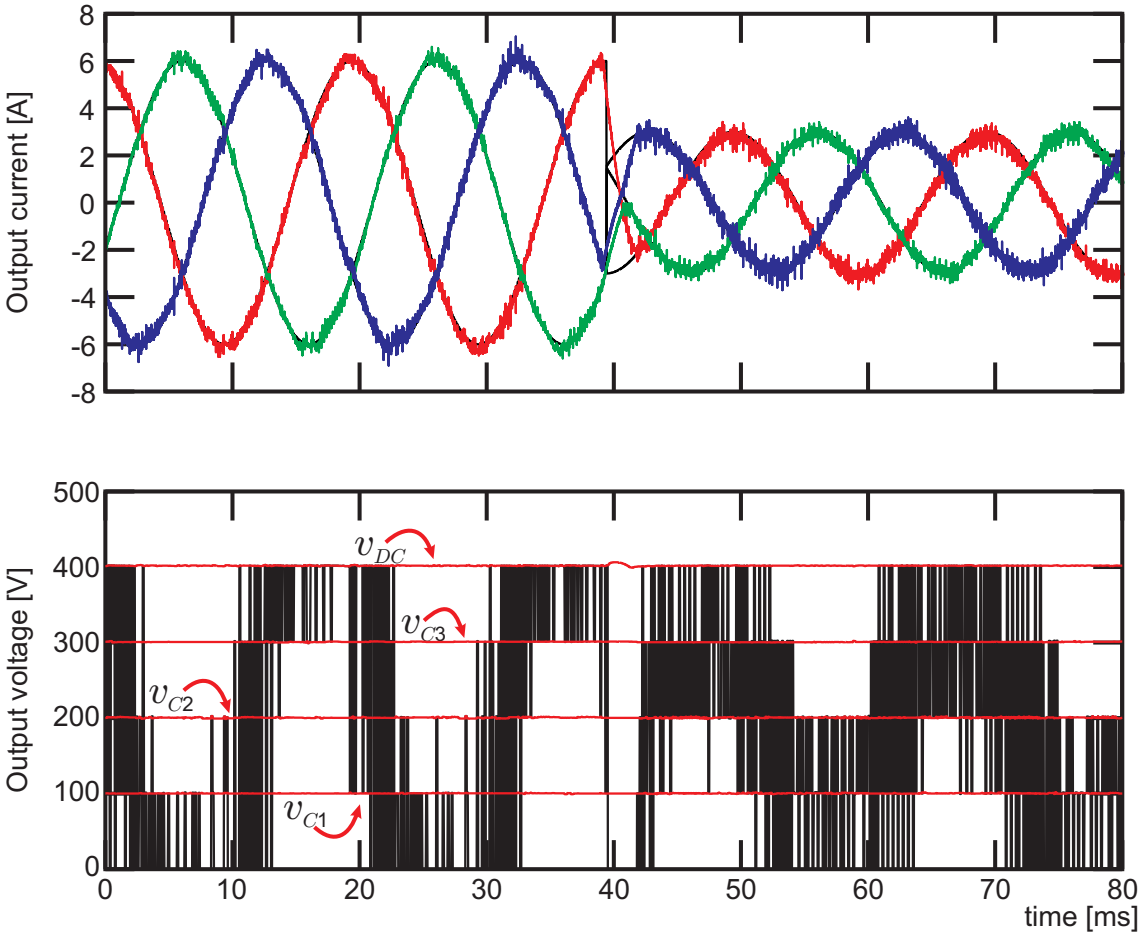


Figure 6.9. *Output current, output voltage and capacitor voltage after a current step.*

Chapter 7

Conclusions and Future Outlook

This dissertation a new multilevel converter topology based on a novel switched DC-cell and variable dc-link operation concept has been proposed. The proposed topology called RMC can be split into two stages: the DC-DC multilevel converter, which is the main contribution of the proposed topology, and the DC-AC output inverter. The RMC can achieve same number of output voltage levels than existing multilevel topologies with a fraction of the active switching devices and capacitors, since the variable dc-link is shared by all output phases of the inverter.

In this dissertation was analyzed an RMC with a 2L-VSI in the DC-AC output inverter, however, it is possible to choose a different DC-AC output inverter, the only condition to change it, it is to use an inverter with a single DC-bus like the NPC, ANPC, T-type, FCC, SMC.

Using a different DC-AC output inverter, RMC will have more numbers of possible switching states, which improve the controller performance and could relax the constraint of the blocking voltages in the power switches.

The main control challenge of the topology is the control of the DC-cell capacitor voltages to generate the desired total number of output levels. Due to the switched DC-cell capacitors, there it is not straight forward to implement a carrier based PWM scheme. This is further complicated by increasing the number of output voltage levels, due the number of possible switching states and redundant states are not enough to achieve a balanced inner voltage using pulse width modulation. For this reason, FCS-MPC was used to verify the performance of the new converter.

At a first glance, the maximum device blocking voltage is the main disadvantage of this topology. However, this is imposed by the selected inverter output stage, which in the case analyzed in this dissertation is a 2L-VSI. This limitation prevents the use of this topology for medium voltage applications. Nevertheless, multilevel converters have now been used extensively in low voltage applications, such as PV inverters, UPS systems, and wind power conversion systems (all below 690 V), due to their power quality, making this topology interesting for further analysis.

In chapter 5 was presented an analysis of the proposed topology in comparison with other topologies for 3-level converters and 5-level converters. The results showed that the proposed topology has a comparable performance in the system variables with the other multilevel converters, achieving sinusoidal output currents, the desired number of output

levels in the voltage, balanced inner voltages, similar THD and spectrum.

In addition, considering the components of the topologies was shown in chapter 5 that the proposed topology has a comparable switching frequency with other multilevel topologies, but fewer power losses, the size of its inner capacitors are comparable with the size of the inner capacitors in the SMC topology. However, the main problem with the proposed topology is the blocking voltage of the output stage power switches, which needs to block full *dc-link*.

Also, in chapter 5 was presented a back-to-back connection of the 3L-RMC, controlling the Torque and Flux in an induction machine, the current in the grid side and the inner voltage in the converter, *dc-link* voltage and flying capacitor voltage. The results presented shows that the back-to-back topology works and it is possible to control the machine side and the grid side with an unique cost function for FCS-MPC.

A laboratory prototype has been built using three shared DC-cells and a three-phase 2L-VSI as inverter output stage. Experimental results show that the DC-cell capacitors can be balanced and controlled accurately while achieving sinusoidal output currents, and a five-level output voltage waveform.

A comprehensive study to determine the most suitable applications for this topology, as well as the evaluation with different output inverter stages (NPC, ANPC, etc.), which could lead to medium voltage operation, is a matter of future research.

Other open problems include the development of a carrier based PWM or space vector modulation strategy for the converter, and more sophisticated FCS-MPC techniques using fixed switching frequency and dv/dt reduction.

Appendix A

Losses calculation

To determine the total power losses (switching and conduction) in the different converters, the thermal tools of PLECS® is used as is shown in Fig. A.1.

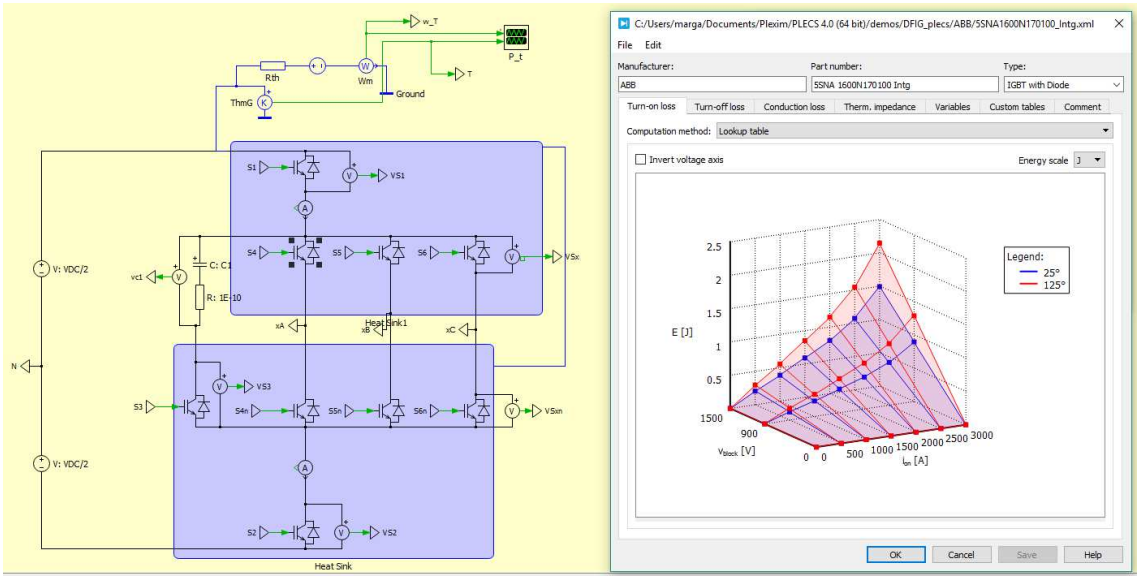


Figure A.1. PLECS® *simulation to calculate total losses of the converter.*

For a fair comparison, the simulation is carried out with the active devices according to the needs in every topology (this is blocking voltage and current rating). The list of commercial devices used in this simulation are shown in Table A.1.

Table A.1
Devices selected

Device name	**cont. Current**	**Voltage**
IRGP4072DPBF	40A	300V
IRG4PC40UDPBF	40A	600V
IRG4PF50WDPBF	30A	900V
IKW40N120H3FKSA1	40A	1200V

Appendix B

Test Bench

The used test bench has been built in the laboratory of the Chair of Power Electronics, Technische Universität Berlin. It includes the power electronic converter and the real-time control system.

Three kW prototype of the proposed multilevel topology was built. The designed converter prototype is shown in Fig. B.1. The area (1) corresponds to the dc-link capacitors, area (2) shows the three DC-cells of the converter, section. (3) shows the variable dc-link bus connection between the DC-cells and the output inverter stage. Finally, area (4) shows the 2L-VSI.

The power switches used in this prototype are Insulated Gate Bipolar Transistors (IGBTs) with freewheeling diode from ON Semiconductor, NGTB30N120IHSWG, with 30A maximum collector current and 1200V blocking voltage. The capacitance of the flying capacitor in all DC-cells is 330μF.

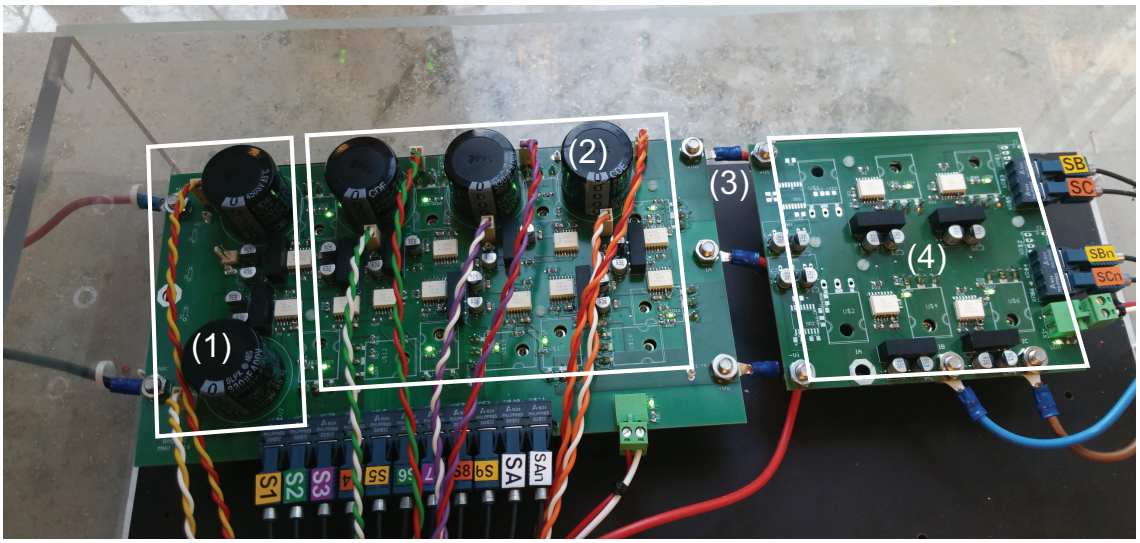


Figure B.1. *RMC prototype: (1) dc-link capacitors; (2) DC-cells; (3) Variable dc-link; (4) 2L-VSI.*

The micro-controller platform used is MicroLabBox from Dspace. This platform has

the following characteristics used in this dissertation: (a) Real-time processor 2 GHz; (b) Programmable FPGA; (c) Analog input 16-bit, $-10..,10V$; and (d) Digital output 5V, 10ns resolution.

Bibliography

[1] D. Krug, S. Bernet, and S. Dieckerhoff, "Comparison of State-of-the-art Voltage Source Converter Topologies for Medium Voltage Applications," in *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, vol. 1, pp. 168–175, IEEE, 2003.

[2] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 5–22, 2005.

[3] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro, "Current-source Converter and Cycloconverter Topologies for Industrial Medium-Voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2786–2797, 2008.

[4] M. Yazdanian and A. Mehrizi-Sani, "Internal model-based current control of the RL filter-based voltage-sourced converter," *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 873–881, 2014.

[5] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters: State of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new Neutral-Point-Clamped PWM inverter," *IEEE Transactions on industry applications*, no. 5, pp. 518–523, 1981.

[7] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 2930–2945, Dec. 2007.

[8] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC'92 Record., 23rd Annual IEEE*, pp. 397–403, IEEE, 1992.

[9] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell Converters: basic concepts and industry applications," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 955–964, Oct. 2002.

[10] G. Gateau, T. A. Meynard, H. Foch, "Stacked multicell converter (SMC): properties and design.," *IEEE 32nd Annual Power Electronics Specialists Conference, PESC 2001.*, June 17-22, Vancouver, Canada. 2001.

[11] E. Babaei, "A Cascade Multilevel Converter Topology with Reduced Number of Switches," *IEEE Transactions on power electronics*, vol. 23, no. 6, pp. 2657–2664, 2008.

[12] G. Adam, I. A. Abdelsalam, K. H. Ahmed, and B. W. Williams, "Hybrid Multilevel Converter with Cascaded H-bridge cells for HVDC applications: Operating principle and scalability," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 65–77, 2015.

[13] M. Schweizer and J. W. Kolar, "High efficiency drive system with 3-level T-type Inverter," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pp. 1–10, IEEE, 2011.

[14] L. Zhe Zhang, O. C. Thomsen, and M. A. E. Andersen, "Discontinuous PWM modulation strategy with circuit-level decoupling concept of three-level neutral-point-clamped (NPC) inverter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1897–1906, 2013.

[15] C. Osawa, Y. Matsumoto, T. Mizukami, and S. Ozaki, "A state-space modeling and a neutral point voltage control for an npc power converter," in *Power Conversion Conference - Nagaoka 1997., Proceedings of the*, vol. 1, pp. 225–230, 1997.

[16] Z. Xiaoming Yuan, H. Stemmler, and I. Barbi, "Evaluation of soft switching techniques for the neutral-point-clamped (NPC) inverter," in *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, vol. 2, pp. 659–664, 1999.

[17] J. D. Barros, J. F. A. Silva, and E. G. A. Jesus, "Fast-predictive optimal control of NPC multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 619–627, 2013.

[18] R. Portillo, S. Vazquez, J. I. Leon, M. M. Prats, and L. G. Franquelo, "Model based adaptive direct power control for three-level NPC converters," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 1148–1157, 2013.

[19] R. Menzies, P. Steimer, and J. Steinke, "Five-level GTO inverters for large induction motor drives," *Industry Applications, IEEE Transactions on*, vol. 30, no. 4, pp. 938–944, 1994.

[20] Q. Song, W. Liu, Q. Yu, X. Xie, and Z. Wang, "A neutral-point potential balancing algorithm for three-level NPC inverters using analytically injected zero-sequence voltage," in *Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE*, vol. 1, pp. 228–233, IEEE, 2003.

[21] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *Power Electronics, IEEE Transactions on*, vol. 15, no. 2, pp. 242–249, 2000.

[22] Sala, R. Salehi, M. Moreno-Eguilaz, M. Salehifar, and L. Romeral, "Clamping diode caused distortion in multilevel NPC full-bridge audio power amplifiers," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, pp. 4941–4948, 2012.

[23] P. Bartolomeüs, P. Le Moigne, and J. Mba, "Over-voltage problems of diode-clamped converters during switchings," in *proc. of the European Power Electronics Conference (EPE'2003)*, 2003.

[24] G. P. Adam, S. J. Finney, A. M. Massoud, and B. W. Williams, "Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi two-state mode," *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 8, pp. 3088–3099, 2008.

[25] G. P. Adam, S. J. Finney, B. W. Williams, and M. T. Mohammed, "Two-level operation of a diode-clamped multilevel inverter," in *Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, pp. 1137–1142, IEEE, 2010.

[26] C. Hochgraf, R. Lasseter, D. Divan, and T. Lipo, "Comparison of multilevel inverters for static var compensation," in *Industry Applications Society Annual Meeting, 1994., Conference Record of the 1994 IEEE*, pp. 921–928, IEEE, 1994.

[27] T. Bruckner, S. Bernet, and H. Guldner, "The active npc converter and its loss-balancing control," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 855–868, 2005.

[28] O. Apeldoorn, B. Odegard, P. Steimer, and S. Bernet, "A 16 MVA anpc-pebb with 6 kA igcts," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 2, pp. 818–824, 2005.

[29] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electronics Specialists Conf. PESC '05*, pp. 2296–2301, 2005.

[30] L. Serpa, P. Barbosa, P. Steimer, and J. Kolar, "Five-level virtual-flux Direct Power Control for the Active Neutral-Point Clamped Multilevel Inverter," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pp. 1668–1674, IEEE, 2008.

[31] S. R. Pulikanti and V. G. Agelidis, "Control of neutral point and flying capacitor voltages in five-level SHE-PWM controlled ANPC converter," in *Industrial Electronics and Applications, 2009. ICIEA 2009. 4th IEEE Conference on*, pp. 172–177, IEEE, 2009.

[32] F. Kieferndorf, M. Basler, L. Serpa, J.-H. Fabian, A. Coccia, and G. Scheuer, "A new medium voltage drive system based on ANPC-5L technology," in *Industrial Technology (ICIT), 2010 IEEE International Conference on*, pp. 643–649, IEEE, 2010.

[33] S. R. Pulikanti and V. G. Agelidis, "Hybrid flying-capacitor-based active-neutral-point-clamped five-level converter operated with SHE-PWM," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4643–4653, 2011.

[34] J. Li, A. Q. Huang, Z. Liang, and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 519–533, 2012.

[35] S. R. Pulikanti, G. Konstantinou, and V. G. Agelidis, "Generalisation of flying capacitor-based Active-Neutral-Point-Clamped Multilevel Converter using Voltage-Level Modulation," *IET Power Electronics*, vol. 5, no. 4, pp. 456–466, 2012.

[36] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-Point Potential Balancing of a Five-level Active Neutral-Point-Clamped Inverter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1907–1918, 2013.

[37] F. Kieferndorf, M. Basler, L. Serpa, J.-H. Fabian, A. Coccia, and G. Scheuer, "ANPC-5L technology applied to medium voltage variable speed drives applications," in *SPEEDAM 2010*, pp. 1718–1725, IEEE, 2010.

[38] www.alstom.com, "Symphony drive line.,"

[39] www.alsintec.com/internacional-en.asp, "ALSTOM VDM6000. Symphony,"

[40] K. Corzine and Y. Familiant, "A new cascaded multilevel h-bridge drive," *IEEE Transactions on Power Electronics*, vol. 17, pp. 125–131, Jan. 2002.

[41] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 21, pp. 140–147, Jan. 2006.

[42] P. Lezana, R. P. Aguilera, and D. E. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 1839–1846, June 2009.

[43] R. H. Wilkinson, T. H. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The general case," *IEEE Transactions on Power Electronics*, vol. 21, pp. 1658–1666, Nov. 2006.

[44] B. Reznikov and A. Ruderman, "Five-level single-leg flying capacitor converter voltage balance dynamics analysis," in *Proc. 35th Annual Conference of the IEEE Industrial Electronics Society - IECON 2009*, pp. 1–6, Portugal, Porto, 3–5 Nov. 2009.

[45] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The general case," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1658–1666, 2006.

[46] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The two-cell case," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1649–1657, 2006.

[47] M. Norambuena, J. Rodriguez, and S. Kouro, "Convertidor Multinivel para el Control y Transmisión de la Energía Eléctrica," Sept. 2016, patent request 201602365.

[48] J. Rodríguez, M. P. Kazmierkowski, J. R. Espinoza, P. Zanchetta, H. Abu-Rub, H. A. Young, and C. A. Rojas, "State of the art of finite control set model predictive control in power electronics," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 1003–1016, 2013.

[49] J. Rodríguez and P. Cortés, *Predictive Control of Power Converters and Electrical Drives.* Wiley, 2012.

[50] E. F. Camacho and C. Bordons, *Model Predictive Control.* Springer, 1999.

[51] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model Predictive Control for Power Converters and Drives: Advances and Trends," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 935–947, Feb. 2017.

[52] J. Zeng, D.-Y. Xue, and D.-C. Yuan, "A multi-model predictive control strategy based on data-centric," in *Natural Computation, 2008. ICNC '08. Fourth International Conference on*, vol. 4, pp. 313–316, 2008.

[53] P. Cortés, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4312–4324, 2008.

[54] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control—a simple and powerful method to control power converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1826–1838, 2009.

[55] J. Rodriguez, J. Pontt, C. A. Silva, P. Correa, P. Lezana, P. Cortes, and U. Ammann, "Predictive current control of a voltage source inverter," vol. 54, pp. 495–503, Feb. 2007.

[56] S. Müller, U. Ammann, and S. Rees, "New time-discrete modulation scheme for matrix converters," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 6, pp. 1607–1615, 2005.

[57] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control& simple and powerful method to control power converters," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 1826–1838, June 2009.

[58] J. Rodriguez, M. P. Kazmierkowski, J. R. Espinoza, P. Zanchetta, H. Abu-Rub, H. A. Young, and C. A. Rojas, "State of the Art of Finite Control Set Model Predictive Control in Power Electronics," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 1003–1016, 2013.

[59] A. Linder and R. Kennel, "Direct model predictive control - a new direct predictive control strategy for electrical drives," in *Power Electronics and Applications, 2005 European Conference on*, 2005.

[60] N. Hoffmann, M. Andresen, F. W. Fuchs, L. Asiminoaei, and P. B. Thogersen., "Variable sampling time finite control-set model predictive current control for voltage source inverters," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, pp. 2215–2222, 2012.

[61] P. Lezana, R. Aguilera, and D. E. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1839–1846, 2009.

[62] C. Ekaputri and A. Syaichu-Rohman., "Implementation model predictive control (MPC) algorithm-3 for inverted pendulum," in *Control and System Graduate Research Colloquium (ICSGRC), 2012 IEEE*, pp. 116–122, 2012.

[63] J. Rodriguez, J. Pontt, P. Cortes, and R. Vargas, "Predictive control of a three-phase neutral point clamped inverter," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, pp. 1364–1369, 2005.

[64] Y.-F. L. W. Zhang, Guang Feng and B. Wu, "A new predictive control strategy for power factor correction," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 1, pp. 403–409, 2003.

[65] M. A. Perez, P. Cortes, and J. Rodriguez., "Predictive control algorithm technique for multilevel asymmetric cascaded h-bridge inverters," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4354–4361, 2008.

[66] R. Kennel and A. Linder, "Predictive control of inverter supplied electrical drives," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, vol. 2, pp. 761–766, 2000.

[67] J. Rodríguez, J. Pontt, C. A. Silva, P. Correa, P. Lezana, P. Cortes, and U. Ammann, "Predictive current control of a voltage source inverter," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 495–503, 2007.

[68] R. Aguilera, P. Lezana, and D. E. Quevedo, "Finite-control-set model predictive control with improved steady-state performance," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 658–667, 2013.

[69] P. Cortes, J. Rodriguez, D. E. Quevedo, and C. Silva, "Predictive current control strategy with imposed load current spectrum," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 612–618, 2008.

[70] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive control of a three-phase neutral-point-clamped inverter," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, pp. 2697–2705, 2007.

[71] P. Lezana, R. Aguilera, and D. Quevedo, "Steady-state issues with finite control set model predictive control," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, pp. 1776–1781, 2009.

[72] R. Aguilera, P. Lezana, and D. E. Quevedo, "A switched model predictive control formulation for flying capacitor converters," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012.