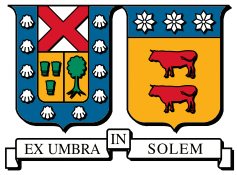

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Hybrid Modulation Strategy for Efficiency Improvement of a Step-Down Partial Power Converter

Francisco Javier González Tijerino

Thesis submitted to the Electronic Department of Universidad Técnica Federico Santa María, as one of the requirements to qualify for the Bachelor's degree as **Ingeniero Civil Electrónico** and the academic Master's degree in **Ciencias de la Ingeniería Electrónica.**

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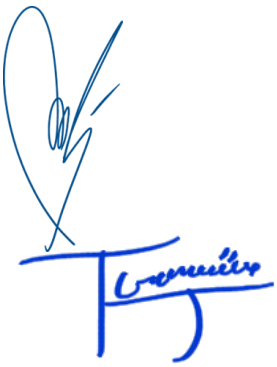

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A mi familia, en la que nací y la que formaré

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Resumen

La electrónica de potencia juega un rol central en la transición energética. Para habilitar la integración de fuentes de energías renovables a las redes eléctricas, o facilitar la electrificación de sectores productivos o aplicaciones domésticas, se necesitan cada vez más convertidores de potencia. Considerando la creciente demanda energética mundial, impulsada por las revoluciones industriales y tecnológicas que suceden cada vez más rápido, se vuelve crucial que los convertidores de potencia sean más eficientes, compactos y flexibles en su operación. Por este motivo, el estudio de los convertidores de potencia parcial (PPC) se ha vuelto más atractivo en los últimos años. Convertidores que procesan solamente una fracción de la potencia en un sistema permiten dispositivos más eficientes y con mejor densidad de potencia. Esto es especialmente positivo en aplicaciones como la electromovilidad o los sistemas de generación de energía solar fotovoltaica domésticos, donde el tamaño de los convertidores son factores de gran importancia.

Enfocándose en la eficiencia y flexibilidad de los PPC, esta tesis presenta una nueva estrategia de modulación híbrida para expandir el rango de operación de un dispositivo. Este enfoque utiliza la estrategia de modulación de corriente principal, con la que normalmente se opera el convertidor, para cierto rango de operación de potencia y, complementariamente, también utiliza una nueva estrategia de modulación propuesta para procesar valores de potencia alejados del nominal. Esto permite expandir el rango de potencia en el que el convertidor opera con eficiencia cercana a la nominal, logrando una mejor utilización del hardware, cambiando únicamente la forma en la que se controlan los interruptores activos del dispositivo.

Para validar la estrategia de modulación diseñada, se realizan pruebas experimentales que muestran la mejora en eficiencia en un rango de operación extendido del convertidor. Además, se estudia a través de simulación, el efecto dinámico de cambiar de modulación mientras el convertidor está en funcionamiento. Ambos resultados confirman la efectividad y factibilidad de utilizar esta novedosa estrategia híbrida de modulación para ampliar el rango útil de operación de un PPC, más allá del punto de operación para el que fue diseñado.

Abstract

Power electronics plays a central role in the ongoing energy transition. To enable the integration of renewable energy sources into power grids and to facilitate electrification of industrial sectors and domestic applications, the demand for power converters continues to grow. Considering the increasing global energy demand, driven by industrial and technological revolutions accelerating, it has become crucial for power converters to achieve higher efficiency, compactness, and operational flexibility. For this reason, the study of Partial Power Converters (PPCs) has gained significant attention in recent years. Converters that process only a fraction of the total system power, allow for more efficient devices with improved power density. This is particularly advantageous in applications such as electric mobility and residential photovoltaic (PV) power generation, where converter size and efficiency are important factors.

Focusing on improving the efficiency and flexibility of PPCs, this thesis introduces a novel hybrid modulation strategy aimed at expanding the operational range of the converter. This approach combines the primary modulation strategy—normally employed in the converter's nominal power range—with a newly proposed modulation scheme designed to process power levels significantly below the nominal value. By doing so, the converter maintains high efficiency across an extended power range, achieving better hardware utilization solely by modifying the control of the active switching devices.

To validate the proposed modulation strategy, experimental tests were conducted demonstrating efficiency improvements across an extended operating range of the converter. In addition, dynamic simulations were performed to analyse the transient behaviour when transitioning between modulation strategies during operation. Both the experimental and simulated results confirm the effectiveness and feasibility of the proposed hybrid modulation strategy in extending the useful operating range of a PPC beyond its nominal design point.

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Abbreviations

AC	:	Alternating Current
BESS	:	Battery Energy Storage System
BO	:	Buck Operation
DAB	:	Dual Active Bridge
DC	:	Direct Current
DPC	:	Differential Power Converter
DPS	:	Double Phase Shift
EPS	:	Extended Phase Shift
EV	:	Electric Vehicle
H2	:	Hydrogen
HF	:	High Frequency
IPOS	:	Input Parallel Output Series
ISOP	:	Input Series Output Parallel
LED	:	Light Emitting Diode
MPPT	:	Maximum Power Point Tracking
PPC	:	Partial Power Converter
PPP	:	Partial Power Processing
PSM	:	Phase Shift Modulation
PV	:	Photo-voltaic
SEPIC	:	Single-Ended Primary Inductor Converter
SiC	:	Silicone-Carbide
SPS	:	Single Phase Shift
SVR	:	Series Voltage Regulator
TPS	:	Triple Phase Shift
ZVS	:	Zero-Voltage Switching

Chapter 1

Introduction

1.1 Background and Motivation

The world is rapidly advancing towards electrification for a greener, more sustainable way of living. The increasing penetration of renewable energy sources and the rapid growth of electrified applications have created new challenges and opportunities for power conversion systems [1]. Modern energy infrastructure, such as photovoltaic (PV) solar energy generation plants, battery energy storage systems (BESS), electric vehicles (EV) charging stations, and electrolysis-based green hydrogen (H2) production, requires highly efficient and flexible power converters to ensure reliable operation under a wide range of operating conditions [2]. In PV-based microgrids, for instance, power converters must cope with large variations in irradiance and temperature, while simultaneously maximizing energy yield and minimizing losses [3]. Similarly, green hydrogen production places stringent requirements on converter efficiency and reliability, since electrolyzers must operate stably to ensure durability [4]. EVs and fast-charging infrastructures present comparable challenges, as converters must achieve both high efficiency and compactness under dynamic load profiles [5].

All of the aforementioned applications operate mainly with direct current (DC), therefore, employing DC-DC converters in the power conversion stage [6]. Traditional DC-DC converter topologies, while well established, can be further enhanced in terms of efficiency and scalability in high-power applications. For example, in PV pre-regulation or battery charging systems, converters must cope with wide input voltage variations and dynamic load profiles [7]. These challenges call for converter architectures that are not only robust and efficient but also capable of adapting their operation dynamically to maximize performance.

Partial power processing (PPP) has emerged as an attractive concept to address these improvement opportunities [8]. Instead of processing the entire system power through a converter stage (Fig. 1.1.a), only a fraction of the total power is handled by the active conversion circuitry (Fig. 1.1.b), leading to potential improvements in efficiency, power density, and cost. Despite their advantages, the performance of Partial Power Converters (PPCs) remains strongly dependent on the modulation strategy employed [9]. Conventional approaches, such as phase-shift modulation (PSM), provide reliable operation and soft-switching capability but suffer from limitations in voltage regulation range and efficiency under low-power conditions [10]. These drawbacks limit their applicability in scenarios where the load profile is highly dynamic or where the converter must operate efficiently across a wide operating range.

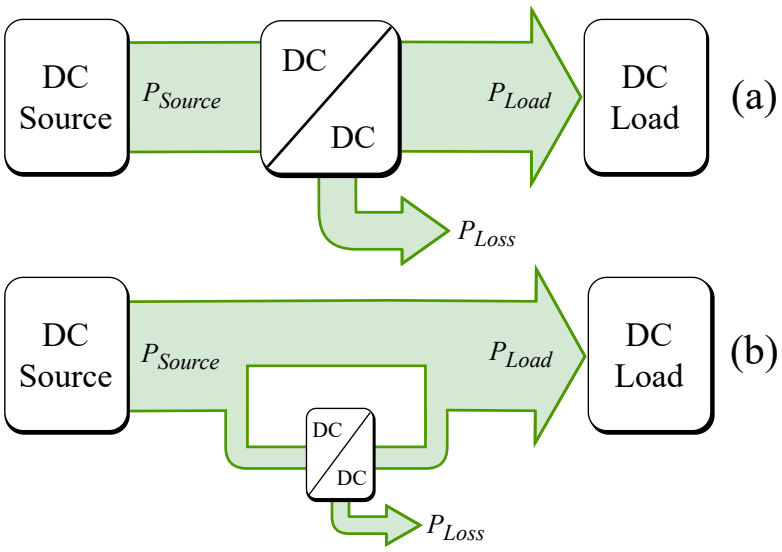


Figure 1.1: Power flow of DC/DC conversion: a) Full Power Converter, b) Partial Power Converter

This context motivates the investigation of alternative modulation strategies that can enhance the operational flexibility of PPCs. The present work explores a new modulation technique that extends the output voltage range and improves efficiency at partial load conditions, while retaining compatibility with the same converter hardware. By enabling reconfiguration of the converter's operating mode, the proposed approach aims to overcome the limitations of conventional PSM and provide a pathway toward higher efficiency and adaptability in power conversion systems.

1.2 Applications of Partial Power Converters

PPCs have attracted increasing attention for the last decade due to their ability to significantly reduce processed power while achieving high overall efficiency. By handling only a fraction of the total system power, PPCs minimize conversion losses, improve power density, and reduce semiconductor stresses, making them highly suitable for applications that demand both high performance and adaptability. These characteristics have positioned PPCs as promising candidates in several key domains of modern energy systems, including PV solar energy generation, BESS, electric mobility, and green hydrogen production [11].

1.2.1 Photovoltaic Solar Energy Generation Systems

PV installations represent one of the most significant application areas for PPCs, and indeed for power electronics as a whole. Variability of irradiance and temperature in PV arrays demands conversion systems that are both efficient and flexible, while minimizing energy losses and operational stress on power devices. PPCs provide an attractive alternative to conventional full-power converters (FPCs). The characteristics stated before make them especially well suited for PV systems, where wide input voltage ranges and highly dynamic operating conditions can occur.

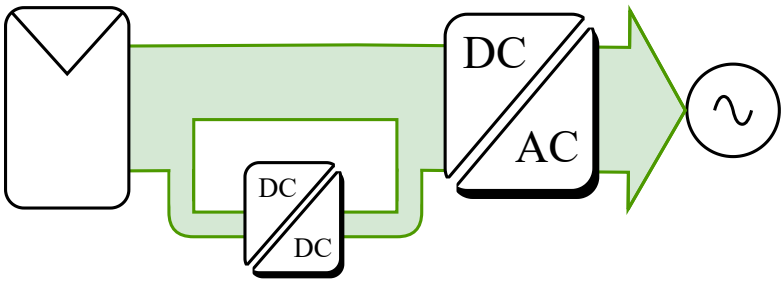


Figure 1.2: Two stage PV architecture with PPC pre-regulator

Two-Stage PV Architectures and Voltage Regulation

In conventional two-stage PV systems, a DC–DC converter is positioned between the PV array and the inverter to regulate the input voltage and decouple the PV operating point and Maximum Power Point Tracking (MPPT) from the DC-link voltage [12]. While effective, full-power intermediate converters add considerable losses and complexity. PPCs address this limitation by processing only a fraction of the PV power, thereby reducing both conduction and switching losses.

Early studies have demonstrated the potential of step-down PPCs integrated into PV string inverters, showing significant reductions in conversion losses and enhanced ability to manage wide voltage variations [13]. More advanced configurations include switched-capacitor-based high step-down PPCs for medium-voltage DC applications, which extend the operational input range and reinforce the scalability of the concept [14]. Furthermore, a series-connected PPC capable of both step-up and step-down operation is proposed in [15], thereby offering superior design flexibility.

PV Power Optimizers

At the module level, PPCs have been integrated to provide localized MPPT. By embedding converters directly at the panel, each module can operate at its individual maximum power point, mitigating issues caused by partial shading or mismatch among panels [16], [17]. This fine-grained control results in superior energy harvesting compared to centralized MPPT schemes.

Recent developments have extended the MPPT range and improved the efficiency of module-integrated PPCs, making them increasingly viable for next-generation PV designs [18]. By reducing mismatch losses and ensuring higher utilization of available solar energy, these converters directly contribute to increasing the total yield of PV installations while maintaining a compact and efficient design.

1.2.2 Battery Energy Storage and Electric Vehicles

Beyond photovoltaic generation, PPCs can also play a key role in applications centered on energy storage and electric mobility. In large-scale BESS, they can be employed to process the imbalance power between interconnected modules [19]. By reducing the circulating currents that typically arise in modular storage architectures, PPCs improve system balancing, increase efficiency, and extend battery lifetime [20], [21]. This functionality is particularly valuable in large installations, where scalability and reliability are paramount.

In the context of electric vehicles, PPCs have been investigated both for charging infrastructure [22] and on-board power management [23], [24]. For fast-charging stations, they offer a means to handle high power levels with reduced conversion losses, thereby enabling shorter charging times and lowering operational costs. Their adaptability to varying battery voltages further supports interoperability across different vehicle platforms, which is essential for the expansion of charging networks.

Within EV powertrains, PPC-based approaches have also been explored to improve the efficiency of on-board converters [24]. Studies highlight that modulation strategies strongly influence both steady-state efficiency and dynamic response, shining light on the importance of control design in these systems [23]. Collectively, these results demonstrate the capacity of PPCs to address critical challenges in electric mobility, from stationary charging infrastructure to on-board energy conversion.

1.2.3 Green Hydrogen Production

The integration of PPCs in hydrogen production systems has emerged as a promising area of research. As renewable-based hydrogen gains importance in the decarbonization of industrial processes, the demand for highly efficient and reliable power converters grows accordingly.An evaluation of the environmental benefits of PV-based microgrids for industrial H2 production is conducted in [25], illustrating the importance of efficient intermediate power conversion stages. Similarly, [4] highlighted the challenges and opportunities of PV-driven hydrogen systems, emphasizing that power electronics play a central role in ensuring both efficiency and operational stability. In this context, PPCs can provide the flexibility required to adapt to the dynamic operating profiles of electrolyzers while maintaining high overall system efficiency [26], [27], [28].

Across these diverse applications, PPCs demonstrate clear advantages over conventional FPCs. By reducing the fraction of power that must be actively processed, PPCs enable higher efficiency, reduced cost, and improved scalability. Whether in PV plants, battery storage systems, EV chargers, or hydrogen production facilities, the capacity of PPCs to adapt dynamically to variable operating conditions makes them a compelling solution for the next generation of sustainable energy systems.

1.3 Overview of DC-DC Converters and Partial Power Processing

1.3.1 Conventional Full Power DC-DC Converters

As introduced in Section 1.1, DC–DC converters play a fundamental role in renewable energy and energy transition applications. These devices transform raw DC power into regulated DC power, enabling control of the output voltage or current according to system requirements. Conventional full-power DC–DC converters are extensively employed in modern commercial and industrial applications, representing a mature and well-established technology.

DC–DC FPCs can be broadly classified into two main categories: non-isolated and isolated [29], [30]. Non-isolated topologies provide direct conversion without galvanic isolation, while isolated converters employ a high-frequency (HF) transformer to introduce an intermediate AC stage, enabling voltage scaling and isolation between input and output. Figure 1.3 summarizes the main topologies identified in the state of the art for this type of converter.

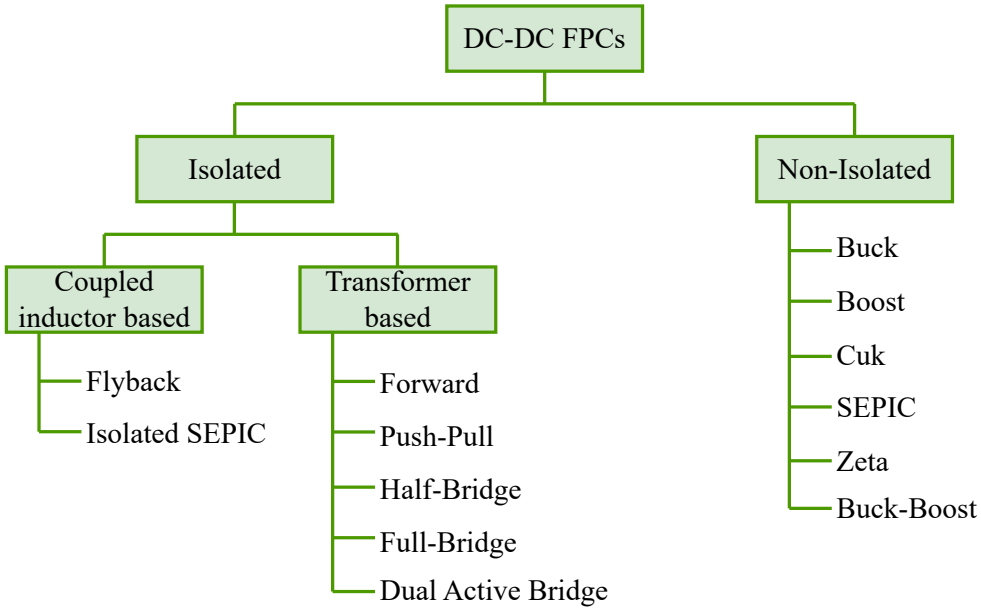


Figure 1.3: Full-Power Converters topologies classification

Non-Isolated

- **Buck:** The buck converter steps down input voltage by periodically connecting the source to the load through a switch and inductor. During the on-time, energy is stored in the inductor while simultaneously supplying the load. During the off-time, the inductor releases stored energy to the load through a diode or synchronous switch. This continuous inductor action smooths current and yields high efficiency [31].

- **Boost:** The boost converter steps up the input voltage by storing energy in an inductor when the switch is on and releasing it in series with the source when the switch is off. This raises the voltage at the output above the input level. The topology is widely applied in LED drivers, renewable energy systems, battery-powered electronics, and power factor correction circuits [31].

- **Cuk:** The Cuk converter transfers energy through a coupling capacitor and provides step-up/step-down capability with inverted output polarity. Two inductors (at input and output) ensure continuous current, while the capacitor handles energy transfer each cycle. This yields low current ripple and improved EMI performance. It is commonly used in applications requiring efficient negative voltage generation or specialized conditioning of DC buses [32].

- **SEPIC:** The SEPIC (Single-Ended Primary Inductor Converter) uses two inductors (or a coupled inductor) and a series capacitor to allow step-up and step-down conversion while maintaining non-inverting output. Energy is stored in the inductors during the switch on-time and transferred to the load via the capacitor during off-time. Its wide input range and continuous input current make it attractive for automotive electronics, PV systems, and battery-powered applications [32].

- **Zeta:** The Zeta converter is the dual of the SEPIC topology, also providing non-inverting step-up/step-down conversion but with continuous input current characteristics. Energy transfer is mediated by a series capacitor, while inductors shape the current at input and output. It is particularly well suited for LED drivers and applications requiring low input current ripple [32].

- **Buck-Boost:** The buck–boost converter provides both step-up and step-down capability, but with an inverted output voltage. Energy is stored in the inductor during switch on-time and released to the output when the switch turns off, similar to the boost process but with polarity inversion. It is simple and compact, used in battery systems and portable devices requiring wide operating ranges.

Isolated

- **Flyback:** The flyback converter is an isolated version of the buck–boost topology, where the transformer operates as a coupled inductor. During the switch on-time, energy is stored in the transformer's magnetizing inductance. When the switch turns off, this stored energy is released to the secondary and delivered to the load through a rectifier [33]. Because of this two-stage storage and transfer process, the flyback is simple and requires no output inductor. It is commonly used in low- to medium-power applications such as AC–DC adapters, auxiliary supplies, and consumer electronics.

- **Isolated SEPIC:** The isolated SEPIC extends the non-isolated SEPIC by replacing the series coupling capacitor with a transformer, which both provides galvanic isolation and allows voltage scaling via the turns ratio. Energy transfer occurs through both an inductor and the transformer, enabling continuous current at both input and output. The topology offers step-up and step-down capability with non-inverting output, making it suitable for wide input ranges in applications such as automotive systems and battery interfaces that require isolation.

- **Forward:** The forward converter transfers energy directly from the input to the output through the transformer while the switch is on, unlike the flyback that relies on energy storage in magnetizing inductance. A demagnetizing winding ensures proper transformer core reset each cycle. Energy not delivered instantaneously is filtered by an output inductor, providing continuous load current. The forward converter achieves higher efficiency than the flyback at medium power levels and is widely used in industrial supplies, telecom equipment, and DC distribution systems [33].

- **Push-Pull:** In the push–pull topology, two switches alternately drive current through opposite halves of a centre-tapped transformer primary [33]. This bidirectional excitation ensures efficient transformer utilization and provides isolation, while the secondary delivers energy to the load through rectifiers and filters. Although efficient at medium power, the topology suffers from unequal voltage stresses and transformer imbalance if care is not taken in design. Push–pull converters are often found in automotive electronics, distributed DC power, and low-cost isolated supplies.

- **Half-Bridge:** The half-bridge converter uses two active switches and a capacitive divider to apply alternating voltages to the transformer primary. Energy is transferred directly during each switch conduction interval, and the secondary provides rectified power to the load [34]. The half-bridge achieves high efficiency, reduces device stress compared to push–pull, and

allows good transformer utilization. It is widely used in medium- to high-power supplies, motor drives, and renewable energy systems.

- **Full-Bridge:** The full-bridge converter employs four switches to apply the full DC bus across the transformer in alternating polarity. This enables maximum transformer utilization and high power transfer capability. Energy flows directly from the DC source through the transformer to the load during each conduction interval, with rectification and filtering on the secondary. Due to its scalability and efficiency, it is widely adopted in high-power applications such as electric vehicle charging, industrial drives, renewable inverters, and datacenter power supplies [33].
- **Dual Active Bridge:** The DAB consists of two full bridges connected by a high-frequency transformer. Both bridges are actively modulated, and power transfer occurs by controlling the phase shift between them [34]. This bidirectional capability allows energy to flow in either direction, while soft-switching (ZVS) can be achieved over a wide operating range, reducing switching losses. The DAB is a leading candidate for high-efficiency, high-power applications such as battery storage interfaces, electric vehicle charging stations, and DC microgrids.

1.3.2 Partial Power Processing

Partial Power Processing (PPP) strategies are generally classified into three categories: **Differential Power Converters (DPCs)**, **Partial Power Converters (PPCs)**, and **Mixed Strategies** [11], [35].

Differential Power Converters are defined as converter architectures intended to correct current imbalances among elements connected in series to a common voltage bus. Unlike conventional converters, they only process the imbalance power, rather than the entire system power [36].

Partial Power Converters, also known as Series Voltage Regulators (SVRs), constitute the main focus of this thesis. PPCs regulate the bulk power flow and voltage levels between the main source and the load of the system. This voltage regulation is achieved by inserting a DC-DC converter in series with either the input or output of the system, such that the generated voltage adds to or subtracts from the input voltage depending on the power flow direction, thus being capable of step-up or step-down operation. With this operating principle, only a fraction of the total system power is processed, resulting in reduced stress on the power stage and potentially higher efficiency.

Finally, Mixed Strategies combine features of both DPCs and PPCs, enabling, for example, simultaneous current balancing and voltage regulation [37]. These approaches often rely on multi-input architectures, such as multi-input DAB, and can achieve very high efficiencies in complex system scenarios.

A key metric in partial power processing is the *partiality ratio* (K_{pr}). This dimensionless parameter is defined as the ratio between the active power processed by the DC-DC regulator and the total active power drawn from the source. The value of K_{pr} depends exclusively on the chosen architecture and on the static voltage gain G_v of the converter. The role and implications of this metric are discussed in greater detail in the following subsection.

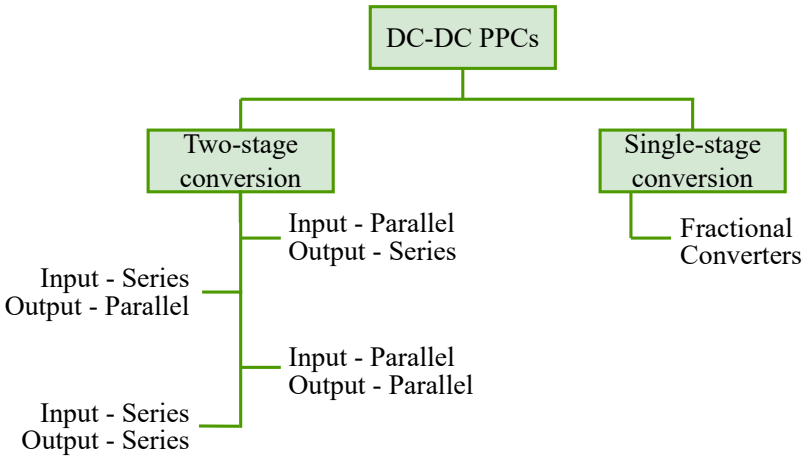


Figure 1.4: Partial Power Converter configurations classification

Classification of PPCs

PPC configurations are commonly classified in the literature as either isolated or non-isolated, depending on whether the associated DC-DC converter includes galvanic isolation through a high-frequency transformer [35]. However, this nomenclature can be confusing, as PPCs themselves cannot provide true galvanic isolation. Even if the converter within the PPC employs a transformer, a portion of the power is transferred directly from the source to the load through the direct path, bypassing the converter. As a result, the overall system does not achieve galvanic isolation.

For this reason, in this thesis, PPC configurations will be classified into configurations that employ single-stage conversion or two-stage conversion, illustrated in Fig. 1.4. Two-stage conversion refers to conversion stages that use an inverter stage and afterwards a rectifying stage. These configurations will not be called "isolated" or "transformer-based", since recent works have proposed two-stage transformerless PPCs, called "AC-link" [38] [39]

Two-stage conversion configurations, which employ high-frequency transformers, coupled inductors or impedance arrays, are the most commonly used PPC configurations [35].

Input-Parallel Output-Series

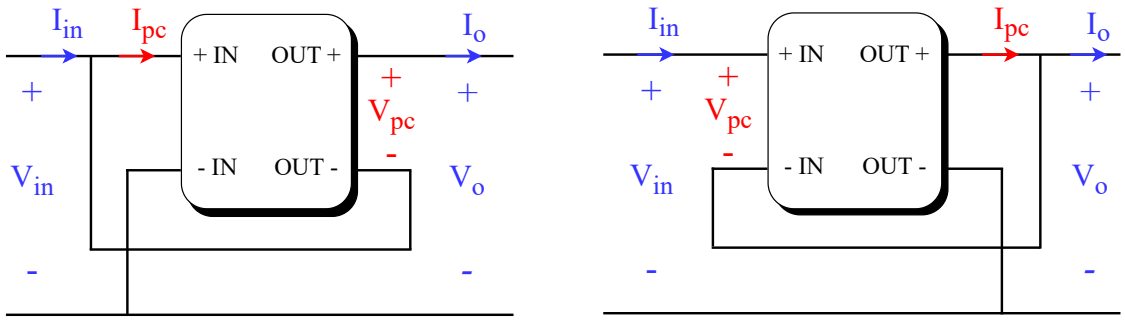
The Input-Parallel Output-Series (IPOS) configuration (shown in Fig. 1.5(a)), also known as Series Regulator Type I, shares both the input voltage (V_{in}) and the output current (I_o) between the converter and the direct path. Its terminal relations are given by:

$$V_o = V_{in} + V_{pc}, \quad I_{in} = I_o + I_{pc}, \tag{1.1}$$

where V_{pc} and I_{pc} are the voltage and current associated with the power converter.

The partiality ratio for this case is:

$$K_{pr_{IPOS}} = 1 - \frac{1}{G_v}. \tag{1.2}$$



(a) IPOS PPC Configuration

(b) ISOP PPC Configuration

Figure 1.5: Most used PPC configurations

Since K_{pr} must be positive, the IPOS configuration is most suitable for step-up applications where $G_v \geq 1$ [40].

The **Input-Series Output-Parallel (ISOP)** configuration (shown in Fig. 1.5(b)), also known as Series Regulator Type II, shares the input current (I_{in}) and the output voltage (V_o) between the converter and the direct path. The terminal relations are defined as:

$$V_o = V_{in} - V_{pc}, \quad I_{in} = I_o - I_{pc}. \tag{1.3}$$

The corresponding partiality ratio is:

$$K_{pr_{ISOP}} = 1 - G_v. \tag{1.4}$$

For K_{pr} to remain positive, this configuration is best suited for step-down applications, where $0 \leq G_v \leq 1$. Variants of the ISOP and IPOS schemes have also been developed to support step-up/down operation [15], [41].

The most common DC-DC converter topologies applied to ISOP and IPOS configurations are Dual Active Bridge, Flyback, Push-Pull, and Full-Bridge converters; all studied in depth in the previous sub-section.

Input-Parallel Output-Parallel and **Input-Series Output-Series** configurations have been found to present operational limitations, which make them unsuitable for practical applications, and are therefore not analysed [35].

Non-isolated PPCs, sometimes referred to as Fractional Power Converters or Fractional Charging Converters, implement PPC concepts using basic topologies such as Buck or Boost. These are possible when the input and output share the same ground potential, reducing complexity and cost. However, their operating range is restricted, typically limited to $0.5 \leq G_v \leq 2$ [42]. Moreover, because internal components may be forced to withstand full system voltage and current, the primary benefit of PPP—reduced component ratings—can be compromised [43]. As a result, non-isolated PPCs are only attractive in niche applications where these constraints can be tolerated.

1.4 Modulation Strategies for PPCs

In this section, the state-of-the-art regarding modulation strategies for PPCs is examined. Throughout the literature review, it was identified that this topic remains relatively under-explored. This gap in research provides the primary motivation for the present work, which focuses on developing and assessing new modulation strategies that may enhance the performance of PPCs. The literature further emphasizes that the selection of a modulation strategy in PPCs is strongly determined by the specific converter topology in use [9]. Among the available approaches, Phase-Shift Modulation (PSM) stands out as the most widely adopted and established technique for active-bridge-based converter topologies. Alternative modulation methods are typically derived from PSM [33], representing variations or extensions aimed at achieving enhanced control performance or addressing specific operational requirements.

Phase-Shift Modulation:

Also known as Single Phase-Shift (SPS), the operating principle and a detailed explanation of this modulation strategy (applied to the selected PPC configuration and topology) are provided in Chapter 2, since PSM is employed as the main benchmark for evaluating the proposed modulation strategies. In essence, PSM consists of introducing a temporal phase shift between the switching signals of two (or more) legs of an active bridge within the converter. This characteristic explains its broad adoption, as it can be naturally applied to both Dual Active Bridge (DAB) converters and full-bridge–based topologies.

The introduced phase shift generates a three-level AC voltage at the bridge output terminals. In most implementations, this voltage is subsequently applied to a high-frequency transformer, as the generated signal typically lies in the tens of kilohertz range or higher. PSM offers several advantages: by producing a three-level waveform, it improves the harmonic quality of the signal processed by the transformer, thereby reducing core-related losses such as hysteresis and saturation. Furthermore, although the active bridge semiconductors switch at the fundamental switching frequency, after rectification the resulting pulsating DC waveform operates effectively at twice that frequency. This behaviour enables the use of smaller magnetic components, such as output inductors, which enhances power density and overall converter efficiency.

Alternative modulations:

In the continuous pursuit of improving PPC operation, alternative modulation strategies have been investigated for different converter topologies. In particular, for DAB-based PPCs, modulation schemes have evolved to allow independent control of the switching actions of the two active bridges. This development has led to three distinct modulation strategies derived from conventional PSM.

- **Dual Phase-Shift Modulation:** Dual Phase-Shift (DPS) modulation introduces a second degree of freedom, typically an inner phase shift angle (D_1, D_2), which controls the duty ratio of one of the H-bridges, creating a three-level AC voltage waveform on that side. The primary objective for employing DPS in high-power PPC applications is the minimization of the inductor and switch RMS current stress for a given target power throughput [44]. Minimizing I_{RMS} is desirable because conduction losses, proportional to I^2R, often dominate the total power losses, especially in high-current, low-voltage designs common in battery integration or energy storage.

The problem with this modulation is the optimal shift angle ratios are determined through a formal mathematical procedure involving the minimization of a Lagrangian function. The objective is to minimize inductor current stress subject to the power transmission constraint. This can require heavy computational effort, thus being useful when extreme efficiency is critical and costs are not an concern.

- **Extended Phase-Shift Modulation:** Extended Phase-Shift (EPS) modulation is closely related to DPS, also combining an inter-bridge phase shift with an inner duty ratio variation. EPS is specifically tailored for maximizing the Zero-Voltage Switching (ZVS) region [45], particularly important in contexts where the converter sees a highly variable voltage conversion ratio.
- **Triple Phase-Shift Modulation:** Triple Phase-Shift (TPS) represents the most advanced and generalized PSM strategy. It offers the maximum control flexibility with three independent variables: the inter-bridge phase shift and two inner phase shifts controlling the duty ratios of both the primary and secondary full bridges [23]. TPS encompasses DPS and EPS as special cases. Its flexibility allows for the concurrent optimization of multiple targets—such as minimizing RMS current stress and ensuring robust ZVS across the entire operating range—often achieved through complex optimization algorithms that manage the inherent trade-off between minimizing conduction losses (requiring lower currents) and maintaining ZVS (requiring a minimum commutation current).

For full-bridge–based converters, the literature review concluded that the only modulation strategy employed is PSM. Although advanced control strategies, such as MPC, can dynamically adjust the switching frequency or the turn-on time of the active switches, the underlying modulation scheme in these control approaches ultimately remains PSM [46].

All of these modulation strategies share a common limitation inherent to the operation of partial power converters: when the processed power decreases, the efficiency correspondingly drops. This behaviour is expected, since both the converter and its modulation scheme are designed to operate optimally around a nominal power point. As the operating point shifts away from this nominal value—particularly toward lower power levels—the efficiency no longer matches the design target. This limitation represents the central motivation for the present study.

1.5 Research Gap and Problem Statement

Conventional modulation strategies for full-bridge-based step-down PPCs, particularly PSM, exhibit reduced efficiency when operating at output power lower than nominal. Additionally, their voltage operation range is limited by the high-frequency transformer turns ratio. The central problem addressed in this thesis is the lack of a modulation strategy for step-down PPCs that simultaneously improves light-load efficiency and broadens the usable output voltage range without requiring hardware modifications.

To address this gap, a new modulation strategy is proposed. Unlike PSM, which introduces a phase shift between the legs of the active bridge, PWM applies identical switching signals to all four switches of the full bridge. This short-circuits the transformer terminals during the active state and effectively reconfigures the converter to operate as a full power converter.

With this newly proposed modulation strategy, a hybrid modulation approach is introduced. It employs PSM when the converter operates at its nominal design power and switches to the new modulation when working at low power levels. This ensures that the system consistently operates with the highest possible efficiency across its entire operating range.

1.6 Objectives and Contributions of this Thesis

1.6.1 General Objective

The general objective is to design and validate a new modulation strategy for a step-down partial power converter, aimed at improving efficiency under low-power operation and extending the voltage regulation range compared to conventional phase-shift modulation (PSM).

1.6.2 Specific Objectives

1. To investigate the state of the art of DC-DC partial power converters and their modulation strategies.
2. To design a novel hybrid modulation strategy for the selected converter topology.
3. To evaluate the proposed strategy through detailed thermal and electrical simulations using PLECS software.
4. To construct a full-bridge step-down partial power converter prototype capable of operating under different modulation strategies.
5. To experimentally validate the proposed modulation strategy using the prototype setup.
6. To compare the performance of the proposed modulation against traditional PSM in terms of efficiency, operating range, and dynamic behaviour.
7. To evaluate the extension of the converter's operating range by combining Pulse Width Modulation (PWM) at light loads with PSM at higher loads, demonstrating their complementary use.

1.6.3 Main Contribution

The main contribution of this thesis is the design and validation of a novel modulation strategy for a step-down partial power converter. The proposed approach reconfigures the converter by applying identical PWM signals to all four active switches of the full-bridge inverter, effectively short-circuiting the transformer and enabling the converter to operate as an equivalent buck converter. This reconfiguration allows the PPC to process the entire system power under light-load conditions, thereby improving efficiency at operating points where conventional phase-shift modulation (PSM) exhibits significant performance degradation.

While PSM provides excellent efficiency at nominal output power, its performance deteriorates as the processed power decreases. By contrast, the proposed Buck Operation shifts the operating point closer to nominal conditions even at reduced load levels, thus maintaining high efficiency. The principal novelty lies in combining both modulation strategies—PSM at nominal or high power levels and PWM at light loads—enabling the converter to adapt dynamically to varying

operating conditions. This complementary use of the two modulations ensures that the PPC consistently operates in a regime that maximizes efficiency across a broad load range.

A secondary but significant contribution of the proposed modulation is the extension of the converter's output voltage range. Since buck operation does not rely on the transformer turns ratio to regulate voltage, it permits operation at output voltages closer to the input, thereby providing greater flexibility and adaptability to different application requirements.

Chapter 2

Converter Topology and Modulation Strategies

Having reviewed the different configurations and topologies within the ample universe of partial power converters, this chapter proceeds by selecting a specific configuration for the case study, namely step-down converters, and then a topology within this configuration. The analysis then focuses on the partiality of the selected converter, identifying where partial power processing occurs and examining the converter's partiality ratio during operation.

With an understanding of the converter established, the discussion moves to the modulation strategies under investigation. First, the well-known phase-shift modulation (PSM) is revisited and analysed in detail, including its equivalent circuits and mathematical analysis. Subsequently, one of the contributions of this thesis is introduced: Buck Operation (BO). A thorough theoretical examination of the proposed modulation is conducted and later, an objective comparison of both strategies is presented, highlighting the respective advantages and limitations of each approach.

2.1 Selected Converter Topology

In order to select the most suitable converter topology for this study, it is first necessary to identify the appropriate PPC configuration. As previously discussed, for step-down operation, the most advantageous configuration is the Input-Series Output-Parallel (ISOP) arrangement. This configuration is illustrated in Fig. 2.1. As shown, the converter voltage V_{pc} is connected in series with the input voltage V_{in}, while the output of the converter is connected in parallel with the overall system output voltage V_o.

The input voltage and current of the system can be expressed as follows:

$$V_{in} = V_{pc} + V_o \tag{2.1}$$

$$i_{in} = i_{pc} - i_r \tag{2.2}$$

Furthermore, the partial power ratio of this configuration is derived in more detail.

$$K_{pr} = \frac{V_{pc} i_{in}}{V_{in} i_{in}} \tag{2.3}$$

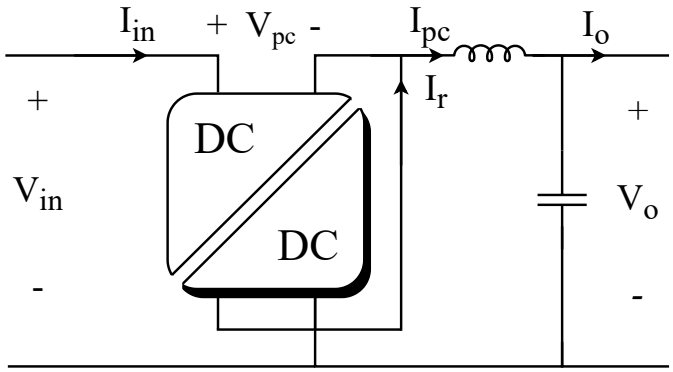


Figure 2.1: Selected step-down PPC configuration

Applying equation 2.1 to equation 2.3, the partial power ratio can be defined in terms of the voltage gain of the converter:

$$K_{pr} = \frac{V_{in} - V_o}{V_{in}}$$
$$K_{pr} = 1 - \frac{V_o}{V_{in}}$$
$$K_{pr} = 1 - G_v \tag{2.4}$$

Having selected the appropriate configuration and analysed its partiality ratio, the next step is to choose the converter topology. For this study, the selected topology is the full-bridge isolated converter. This topology employs a full-bridge active inverter stage and a full-bridge diode rectifier stage, which are interconnected through a high-frequency transformer. An LC filter is placed at the rectifier output to reduce voltage ripple and deliver a smoother DC output.

This topology was selected because the literature review showed that DAB-based PPCs have been extensively studied, with multiple PSM variations developed to enhance their performance. In contrast, the modulation of full-bridge-based PPCs is largely limited to the Single Phase Shift (SPS) scheme, making this topology more open to innovation and research in advanced modulation strategies.

The complete circuit diagram of this topology is shown in Fig. 2.2. The diagram illustrates the input voltage V_{in}, the converter voltage V_{pc}, and the output voltage V_o, as well as the transformer primary and secondary voltages, denoted as v_1 and v_2. The rectifier output voltage is represented as V_r. The corresponding currents are also identified: the input current I_{in}, the rectifier output current I_r, the converter current I_{pc}, and the load output current I_o. Additionally, the transformer primary and secondary currents are indicated as i_1 and i_2.

The power semiconductors of the full-bridge inverter are labelled as S (S_a, S_b, S_c, and S_d), while the rectifier diodes are labelled as D (D_a, D_b, D_c, and D_d). Finally, the elements of the output filter are denoted as L_o and C_o.

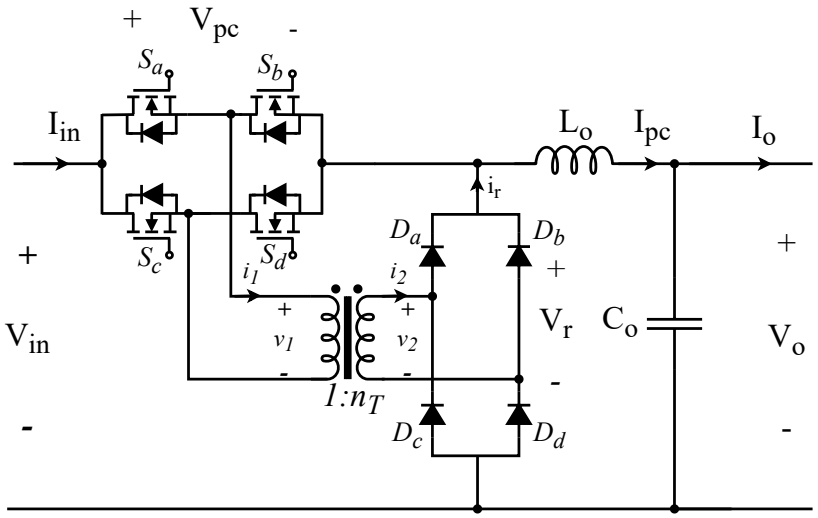


Figure 2.2: Selected full-bridge-based step-down PPC topology

In this converter, partiality does not imply the existence of a literal "100% efficient wire" transmitting part of the power while only the remainder is processed by the converter. Instead, the converter conducts the full system current, but generates at its terminals a voltage lower than the input voltage. This generated voltage, which is subtracted from the input voltage to regulate the output, is where the partiality arises. As a result, the converter effectively processes only a fraction of the power, even though it handles the total current.

The operating principle and transfer function of the converter are determined by the modulation strategy used to control the switching of the active bridge semiconductors. This constitutes the central focus of the present work. Since semiconductor devices represent the primary source of power losses, the manner in which they are driven is crucial in determining the overall efficiency of the system.

2.2 Modulation Strategies for the Selected Topology

In the modulation strategy for this topology, the objective is to generate an AC waveform at the output of the active bridge by introducing a phase shift between the inverter legs. This alternating signal, which may be two or three-level waveforms (for a two-leg inverter), is then transferred through the high-frequency transformer to step up or step down the voltage level, and subsequently rectified by the diode bridge.

The following sections provide a detailed analysis of the most widely used modulation strategy, phase-shift modulation, and introduce a complementary alternative.

2.2.1 Phase-Shift Modulation

As discussed in the literature review presented in Section 1.4, the most widely adopted modulation strategy for partial power converters based on full-bridge is phase-shift modulation (PSM). The operating principle of this strategy is illustrated in Fig. 2.3. It is important to note that the

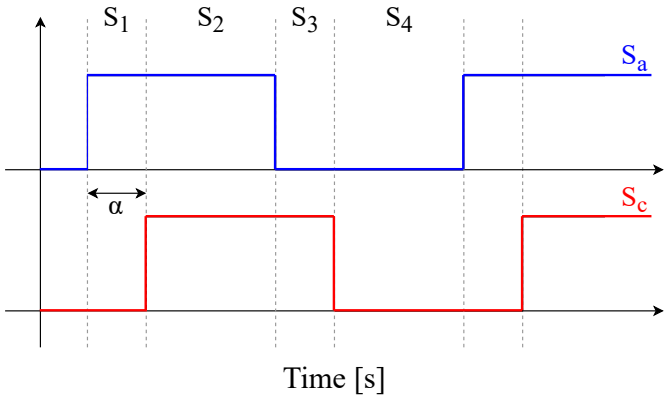


Figure 2.3: Phase-shift Modulation

figure depicts the switching signals of switches S_a and S_c, while S_b and S_d are driven in a complementary manner to S_a and S_c, respectively. As shown, a phase shift—denoted as α and expressed in radians—is introduced between the gating signals of the two inverter legs. This phase displacement results in four distinct conduction states in the converter, labelled S_1, S_2, S_3, and S_4.

Fig. 2.4 shows the equivalent circuits corresponding to each conduction state:

- S_1: Shown in (a), this state happens when S_a is ON and S_c is OFF. During this conduction state and in steady state, the voltage on the primary side of the HF transformer $v_{1_{S_1}}$ is given by:

$$v_{1_{S_1}} = V_{in} - V_r \tag{2.5}$$

  Furthermore, in this state, $V_{r_{S_1}} = v_2$, thus the following can be affirmed:

$$V_{r_{S_1}} = n_T(V_{in} - V_{r_{S_1}})$$

$$V_{r_{S_1}} = \frac{n_T V_{in}}{1 + n_T} \tag{2.6}$$

- S_2: Shown in (b). In this conduction state, both S_a and S_c are ON. During this state, the primary side of the transformer is short-circuited, thus equal to zero. While this happens, voltage on the diode rectifier, V_r is also zero, but the four diodes conduct current stored in the inductor.

- S_3: Shown in (c). This states is complimentary to S_1, meaning that in this case, S_a is OFF and S_c is ON. Given the switches conducting, voltage on the primary side of the transformer is given by.

$$v_{1_{S_3}} = V_r - V_{in} \tag{2.7}$$

  Analysis for S_1 help deduct that in this conduction state, $V_{r_{S_3}}$ is:

$$V_{r_{S_3}} = -\frac{n_T V_{in}}{1 + n_T} \tag{2.8}$$

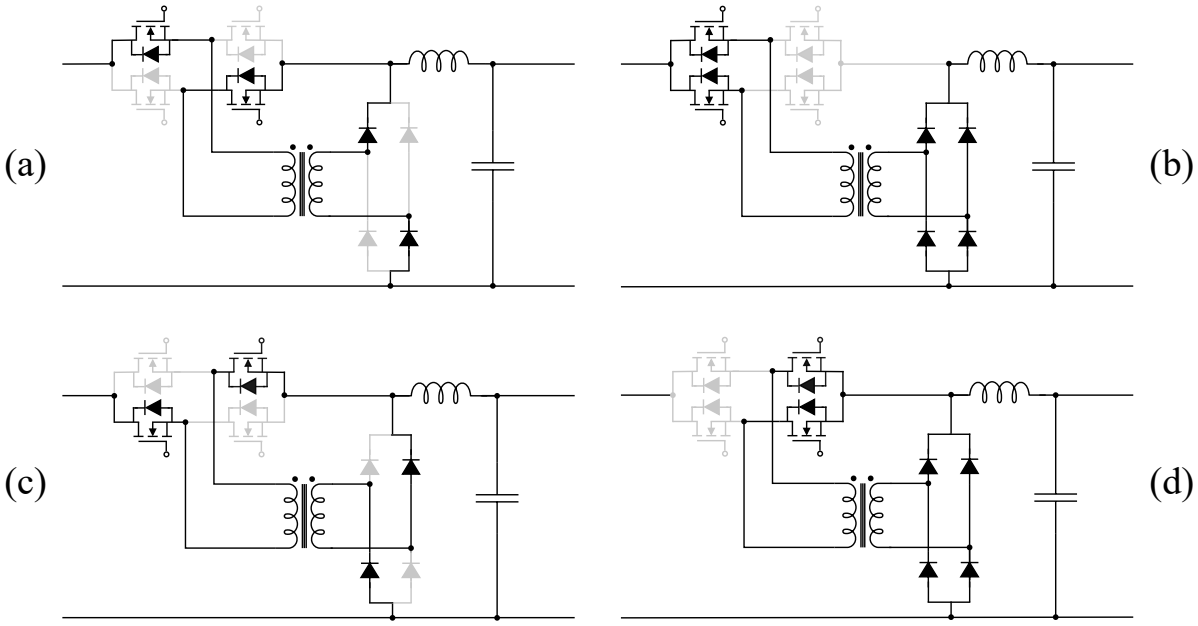


Figure 2.4: Equivalent circuits of PSM operation states. (a) S_1, (b) S_2, (c) S_3, (d) S_4

Table 2.1: Conduction states for Phase-Shift Modulation

State	Active Bridge				Diode Bridge			
S_1	S_a	-	-	S_d	D_a	-	-	D_d
S_2	S_a	-	S_c	-	D_a	D_b	D_c	D_d
S_3	-	S_b	S_c	-	-	D_b	D_c	-
S_4	-	S_b	-	S_d	D_a	D_b	D_c	D_d

- S_4: Shown in (d). Finally, in this state, both S_a and S_c are OFF. This state's operation is the same as S_2.

Having studied the steady-state behaviour of the converter under the different conduction states generated by PSM, the voltage gain of the converter operating with this modulation strategy is deduced. The output voltage of the system V_o is generated by the pulsating DC signal V_r, passing through the LC filter. Thus V_o in steady state is equal to the mean value of V_r. This can be calculated as the amplitude of the signal multiplied by its duty cycle. The duty cycle of V_r is given by the phase shift between legs of the inverter: α/π.

$$V_{o_{PSM}} = \frac{n_T V_{in}}{1 + n_T} \frac{\alpha}{\pi} \tag{2.9}$$

And the voltage gain is finally expressed as:

$$G_{v_{PSM}} = \frac{\alpha n_T}{\pi(1 + n_T)} \tag{2.10}$$

The partiality ratio of the converter under this modulation strategy is expressed in terms of α and n_T:

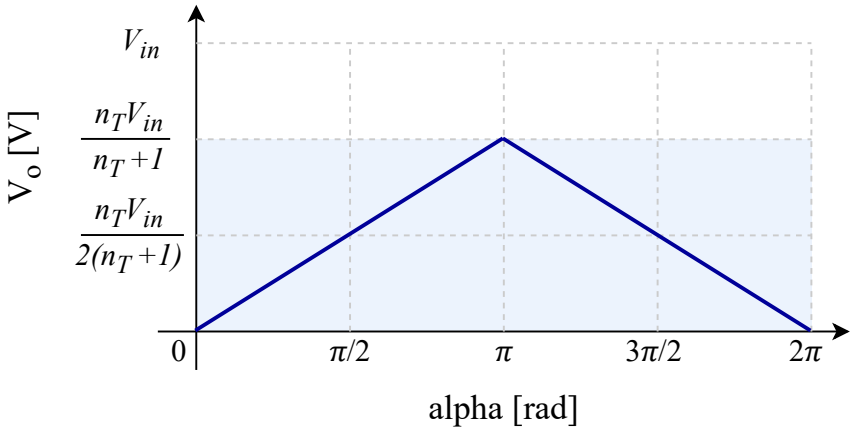


Figure 2.5: Output voltage operation range of the converter under Phase-Shift Modulation

$$K_{pr_{PSM}} = \frac{\pi + n_T(\pi - \alpha)}{\pi(1 + n_T)} \tag{2.11}$$

This result indicates that for a bigger phase shift between inverter legs, the fraction of power being processed by the converter will be smaller, thus gaining higher overall system efficiency.

Expanding the analysis of PSM, the output voltage operating range achievable by the converter is examined. As shown in Fig. 2.5, the output voltage depends directly on both the phase shift between the inverter legs and the transformer turns ratio. Two main observations can be drawn from the figure. First, as the phase shift increases, a point is reached where the output voltage no longer rises linearly. This occurs because phase shifts greater than π effectively correspond to negative phase shifts. The second key observation is that, when operating under PSM, the converter can never achieve an output voltage equal to the input voltage. The attainable output voltage is strictly dependent on the transformer turns ratio. Achieving an output voltage very close to the input would require an infinite turns ratio, which is not achievable in practice.

To finalize the study of the converter operating with PSM, efficiency is analysed. For this, a thermal simulation was conducted using PLECS software. Thermal losses of the semiconductor devices were modelled using realistic thermal models provided by manufacturers. The thermal model used for the active switches is that of Infineon's *FF33MR12W1M1HP_B11* SiC MOSFETS. For the diodes, Infineon's *IKW75N65EH5* diode thermal model is used. Transformer losses were excluded from simulation efficiency calculations, focussing on semiconductor and control losses to establish a theoretical baseline. In practice, these losses include: Core hysteresis (energy dissipation from magnetic domain reversal, reducing efficiency at high flux densities), core eddy currents (resistive heating from induced currents, scaling with frequency squared and prominent at high switching rates), winding DC resistance (I^2R ohmic losses, dominant at high currents), skin effect (current surface crowding, increasing effective resistance at high frequencies), and proximity effect (additional eddy currents from adjacent windings, exacerbating AC resistance in compact designs)—contribute significantly, often accounting for 80-90% of total dissipation [47].

The passive components used in the prototype—namely the output inductor and capacitor—were selected based on standard ripple constraints for current and voltage in partial power converter

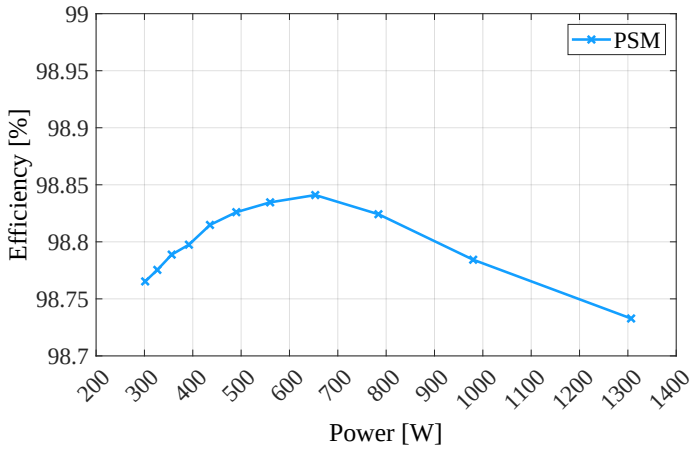


Figure 2.6: Efficiency curve of the converter using PSM

architectures. In phase-shift modulation (PSM), the effective duty cycle of the pulsating voltage applied to the LC filter is related to the phase-shift angle between the full-bridge legs according to

$$d = \frac{\alpha}{\pi},$$

where α is the phase displacement. Furthermore, although each semiconductor device switches at frequency f_s, the bipolar switching pattern of the full-bridge produces a pulsating waveform at the filter input with a fundamental frequency of $2f_s$. Therefore, the filter must be designed using $2f_s$ as the effective switching frequency.

For a given allowable peak-to-peak inductor current ripple ΔI_L, the inductance required to limit this ripple is given by

$$L \geq \frac{(V_{\text{in}} - V_o)\, d}{\Delta I_L\, (2f_s)}. \tag{2.12}$$

Similarly, the output capacitor value required to maintain the desired peak-to-peak voltage ripple ΔV_o can be expressed as

$$C \geq \frac{\Delta I_L}{8(2f_s)\Delta V_o}. \tag{2.13}$$

In practice, the values implemented in the prototype (L = 1.2 mH and C = 500 μF) were chosen from available laboratory components that satisfy these design constraints, ensuring acceptable output current and voltage ripple given the switching frequency and operating range of the converter.

Simulation parameters are shown in Table 2.2. A schematic of the thermal and electrical simulation is included in Appendix B.

Fig 2.6 shows the efficiency results computed by the simulation. It can be observed that efficiency at low output power is lower than at the nominal operating range. In reality, this difference is more notorious, since when processed power is inferior to the partiality ratio the converter was designed for, transformer losses impact efficiency more.

This insight, in addition to the limited output voltage operating range, motivates the search for complementary modulation strategies that further enhance the performance of the converter.

Table 2.2: Simulation parameters

Parameter	Value	Unit
Input Voltage V_{in}	400	V
Switching Frequency f_{sw}	20	kHz
Transformer Turn Ratio n_T	0.6	–
Output Inductor L_o	1.2	mH
Output Capacitor C_o	500	μF

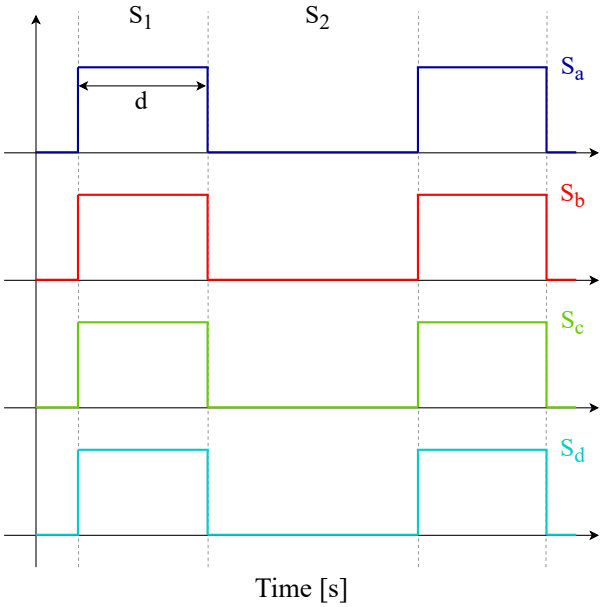


Figure 2.7: Buck Operation

2.2.2 Proposed Buck Operation

One of the main contributions of this thesis is presented in this section. It consists of a novel modulation strategy for the selected topology. The central idea is to commutate all four switches of the active bridge synchronously using pulse-width modulation (PWM). This principle is illustrated in Fig. 2.7, where it can be observed that all semiconductor devices switch simultaneously.

This method of modulating the converter is distinctive for several reasons. First, commutating both devices of the same leg simultaneously is typically considered a prohibited state, as it risks short-circuiting the decoupling capacitor that is commonly connected in parallel with the active bridge. For this reason, when selecting the topology for this work, the decoupling capacitor was intentionally removed. Moreover, in this case, not only are the two devices of each leg switched together, but the entire active bridge is commutated synchronously. This operation fundamentally changes the typical behaviour of the circuit, since the terminals of the high-frequency transformer are short-circuited, rendering the transformer unused throughout the converter's operation.

This phenomenon is illustrated in Fig. 2.8. As shown in (a), during the conduction state S_1, all four switches of the active bridge are turned ON, which short-circuits the transformer primary and prevents the diode bridge from conducting. Conversely, in (b), during the conduction state S_2, all four active switches are OFF, allowing all four diodes of the uncontrolled rectifier bridge to

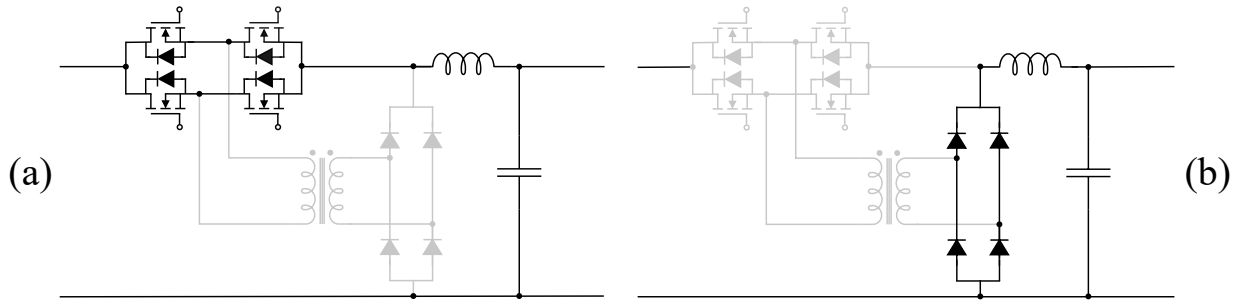


Figure 2.8: Equivalent circuits of BO operation states. (a) S_1 (b) S_2

Table 2.3: Conduction states for Buck Operation

State	Active Bridge				Diode Bridge			
S_1	S_a	S_b	S_c	S_d	-	-	-	-
S_2	-	-	-	-	D_a	D_b	D_c	D_d

conduct simultaneously. This behaviour effectively transforms the circuit into an equivalent buck converter, where instead of a single active switch and diode, four active switches and four diodes are employed.

Another distinguishing feature of this modulation strategy is that, under this mode of operation, the circuit no longer functions as a partial power converter. On the contrary, the converter processes the entire system power. At first thought, this may appear counter-intuitive, given that much of the work thus far has emphasized the advantages of partial power processing. However, this research has identified several reasons why this alternative mode of operation may be attractive and worthy of investigation.

The first motivation is the expansion of the output voltage operating range. As shown in Fig. 2.9, this strategy allows the converter to achieve higher output voltages than those attainable under PSM. This is because the operating principle of the converter using PWM does not depend on the high-frequency transformer; instead, its voltage gain follows that of a conventional buck converter, determined solely by the duty cycle of the PWM control signal. With this, the output voltage of the converter operating with PWM $V_{o_{PWM}}$ can be determined as:

$$V_{o_{PWM}} = dV_{in} \tag{2.14}$$

Thus, the voltage gain is equivalent to the duty cycle d. This provides the converter with a higher degree of independence and enables an expanded operating range suitable for applications that demand it. The partiality ratio calculated for PSM is not applicable in this case, since the converter is processing the full power of the system. In other words, the partiality ratio would be 100%.

A second motivation is related to efficiency under varying load conditions. When operating with PSM, the converter exhibits reduced efficiency at low power since it is underutilized and departs from the nominal operating point for which it was designed, as explained in the previous sub-section. In contrast, when the application demands lower power, the modulation strategy can be switched to PWM, forcing the converter to process the entire system power and effectively

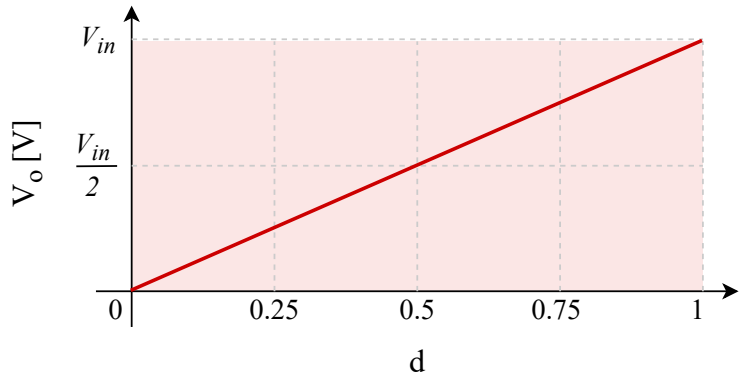


Figure 2.9: Output voltage operation range of the converter under Buck Operation

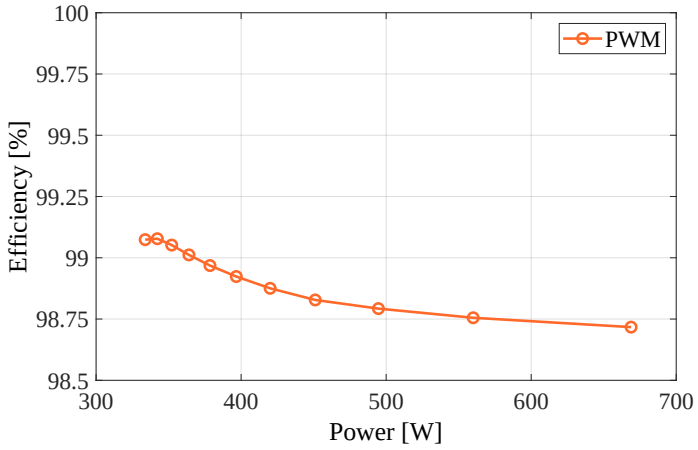


Figure 2.10: Efficiency curve of the converter using BO

bringing it closer to its nominal operating point. This results in an efficiency level consistent with the converter's intended design. This is shown in Fig. 2.10. A notable fact about these simulation efficiency results is that the power range of the experiment is considerably lower than the results shown in Fig. 2.6. This is because, with PWM, the converter processes the full system's power, thus being able to achieve lower output power.

This motivation was the primary reason for designing and studying the proposed modulation strategy, and it ultimately led to the development of the hybrid operation approach, which will be introduced in the next chapter.

2.2.3 Comparative Theoretical Analysis

Having presented both modulation strategies, the next step is to compare their operation in order to identify key differences and establish under which conditions each is most advantageous. The four main points to be compared are Power Processing, Key Operation Signals, Device Stress, and Efficiency Profiles for both modulations.

Power Processing

One of the fundamental differences between Phase-Shift Modulation and PWM lies in how the converter processes power. Under PSM, the converter operates as a partial power processor: the full input current flows through the active bridge, but the voltage it generates is only a fraction of the input, subtracting from the system input to regulate the output. As a result, only a portion of the total system power is actively processed by the converter. This characteristic is what gives PPCs their efficiency advantage at nominal operating conditions.

In contrast, under BO, the converter no longer behaves as a partial power processor. By synchronizing all four switches and short-circuiting the transformer's terminals, the entire system power is processed through the active bridge and diode rectifier, just as in a conventional buck converter. At first, this appears to contradict the philosophy of partial power processing. However, it becomes advantageous under light-load conditions, where the converter would otherwise be underutilized and less efficient in PSM mode. In this scenario, BO restores the system to full-power processing, maintaining effective utilization of the converter hardware.

Output Voltage Operating Range

In the case of PSM, as explained in sub-section 2.2.1, the output voltage operating range is inherently constrained by the design of the high-frequency transformer. This limitation, combined with the fact that the phase shift angle α is restricted to values between 0 and π, significantly reduces the flexibility of the converter. In practice, it is also not advisable to operate with output voltages that are too low relative to the input, since the semiconductors must block higher voltages, increasing device stress and degrading efficiency.

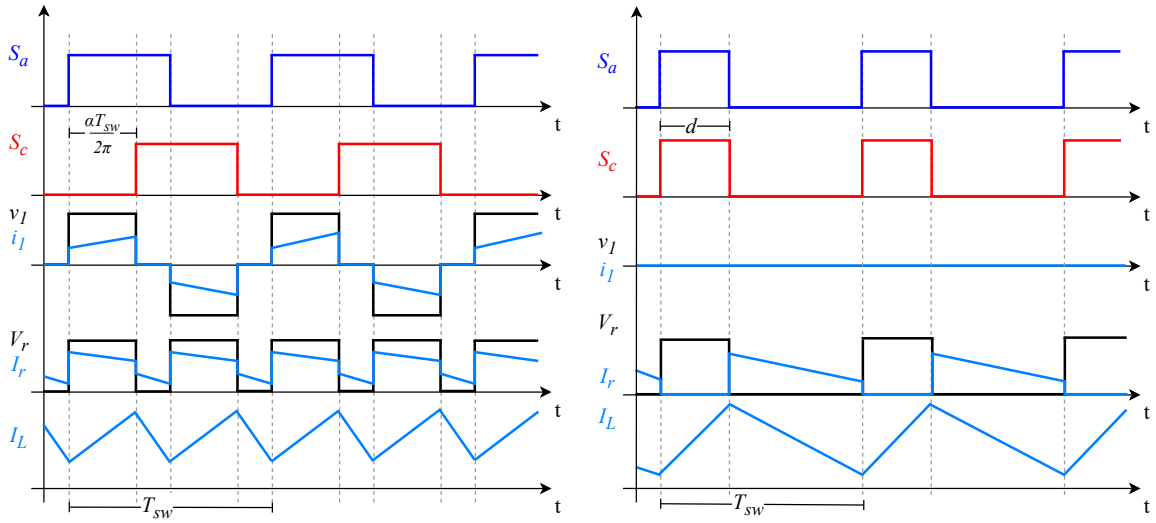
PWM achieves a much wider output voltage operating range. Its main advantage lies in the fact that it is not dependent on the transformer design. By reconfiguring the converter operation through software, an alternative operating mode is enabled, allowing output voltages to reach values much closer to the input. The higher the output voltage—that is, the less voltage reduction performed by the converter—the lower the stress on the semiconductors and, consequently, the higher the overall efficiency.

Key Operation Signals

Figure 2.11 shows the main waveforms of the converter operating under both modulation schemes.

The first and most evident difference lies in the voltage and current across the transformer. Under PSM, the transformer voltage exhibits a three-level AC waveform generated by the phase shift between the inverter legs, as previously explained. This waveform is then rectified by the diode bridge, producing a pulsating DC voltage at twice the switching frequency of the active bridge. The effective duty cycle of this voltage is directly determined by the phase shift angle α. Consequently, the inductor current also shows a ripple component at twice the switching frequency, with a relatively small amplitude.

In contrast, the converter signals under PWM differ significantly. The transformer voltage is effectively zero at all times, since its terminals are permanently short-circuited during operation. The voltage at the diode bridge—which in this case behaves as a single equivalent diode—remains pulsating DC, but at the same frequency as the switching frequency of the active devices. The duty cycle of this voltage is set directly by the duty cycle of the PWM control signal. As a result, the



(a) Phase-Shift Modulation (b) Pulse-Width Modulation

Figure 2.11: Key Operation Signals

output inductor must handle a larger current ripple component at a lower frequency compared to PSM operation.

Device Stress

Another key difference arises in the electrical stress imposed on the semiconductor devices. In PSM, voltage and current stresses are moderated by the partial power processing principle. Since only a fraction of the total power is actively handled, semiconductor currents remain relatively small, and the transformer helps distribute voltage stress.

By contrast, in BO, all of the system power flows through semiconductor devices. This increases the current stress on both switches and diodes compared to PSM operation. The increased stress does not necessarily compromise converter reliability, but it does highlight the importance of carefully selecting semiconductor devices capable of handling the higher current levels. This increased stress is the main reason why BO is applicable only with light loads.

Efficiency Profiles

The distinct power processing paths of PSM and PWM directly shape their efficiency characteristics across the load range. PSM typically achieves very high efficiency close to nominal load, where the fraction of power processed is minimized. However, as the load decreases, the efficiency drops. This reduction arises because the converter continues to incur fixed switching and conduction losses even though the amount of power it actively processes becomes very small relative to the total, resulting in poor utilization of the conversion stage.

On the other hand, BO forces the converter to process the entire system power, which would normally be considered less efficient, yet at low loads this reconfiguration proves beneficial: the converter is once again operating near its designed power handling point, and its relative efficiency

improves compared to PSM in the same conditions. The complementary nature of these two profiles suggests that a hybrid control strategy, employing PSM at higher loads and PWM at lighter loads, can achieve consistently high efficiency across the full operating range.

This comparative analysis gives the information needed to design a hybrid modulation strategy that utilizes each modulation when it is more suitable in terms of efficiency. This might help achieve near-to-peak efficiency over a wider operational range.

Table 2.4: Summary of comparative analysis between modulation strategies

Comparison Point	PSM	PWM
Power Processing	Partial power processing	Full power processing
Output Voltage Operating Range	Dependant of transformer design and constrained by phase shift between 0 and π.	Not dependant of transformer and permitting output voltage very close to input.
Key Operation Signals	v_1 is three-level AC. V_r duty cycle given by α; frequency double of switching freq. I_L frequency double of switching freq. and lower amplitude than PWM.	v_1 is zero. V_r duty cycle given by d and frequency equal to switching freq. I_L frequency equal to switching freq. and higher amplitude compared to PWM.
Device Stress	Lower voltage stress due to partial power processing.	Higher current stress since all power flows through switches and diodes.
Efficiency Profiles	High efficiency at nominal load, but efficiency decreases sharply at light load.	Superior efficiency at light load by restoring operation closer to nominal conditions.

2.3 Chapter Summary

This chapter presents the selected configuration and topology for the partial power converter (PPC) under study, focusing on a step-down Input-Series Output-Parallel (ISOP) arrangement with a full-bridge isolated converter. The partial power ratio is derived and analysed, highlighting its role in efficiency optimization. Traditional phase-shift modulation (PSM) is reviewed in detail, including equivalent circuits, conduction states, voltage gain, efficiency profiles from simulation experiments and operational limitations, such as dependency on the transformer turns ratio and reduced efficiency at light loads.

A novel Buck Operation (BO) strategy is proposed, involving synchronous switching of all active bridge semiconductors to emulate a Buck converter, resulting in full power processing and an expanded output voltage range independent of the transformer. A comparative theoretical analysis between PSM and PWM is conducted, evaluating differences in power processing, key operation signals, device stress, and efficiency profiles, demonstrating complementary strengths: PSM excels at nominal loads, while BO improves efficiency at lighter loads.

Chapter 3

Hybrid Modulation Strategy

With a detailed understanding of the converter's operation under both PSM and PWM, a hybrid modulation strategy can now be introduced. This approach combines the two modulation methods at different operating points in order to ensure that the converter maintains high efficiency across a wider load range. As demonstrated in simulation results presented in the previous chapter, PSM achieves excellent efficiency near nominal load. However, efficiency decreases as the output power drops below the nominal point. In contrast, when the same converter operates under BO, efficiency is higher at these lower power levels.

The central idea of the hybrid strategy is rooted in how PPCs are designed. When a partial power converter is engineered, all of its components—including semiconductors, passive elements, and the transformer—are sized for a specific design point corresponding to the nominal processed power. In practice, though, many applications feature variable load profiles, such as energy storage systems with dynamic charge/discharge cycles or PV installations subject to changing irradiance. Under these conditions, the load power often falls below the nominal value. As this happens, the converter operating with PSM moves away from its design point, and efficiency begins to degrade.

The hybrid strategy addresses this challenge by switching to PWM once the load power drops below the nominal level associated with the converter's partiality ratio. In buck mode, the converter processes the entire system power, effectively bringing the operating point closer to the nominal processing level and recovering the efficiency that would otherwise be lost. This approach ensures that the converter continues to operate near its optimal design point, even as the load varies.

Care must be taken, however, when performing this transition. Since the converter components were sized for a maximum processed power, switching to buck mode requires careful monitoring to ensure that these limits are not exceeded. Otherwise, excessive stress on the semiconductors, passive elements, or transformer could compromise reliability.

Figure 3.1 provides a theoretical illustration of the efficiency curves for PSM, PWM, and the hybrid modulation strategy. It can be observed that the efficiency of PWM peaks at lower output power levels, while PSM maintains superior efficiency at or near nominal load. The hybrid strategy seeks to switch between the two precisely around the partiality ratio, which—as discussed earlier—represents the fraction of total system power that the converter is designed to process. Thus, when the load demand falls below this design threshold, the converter transitions to PWM, ensuring operation remains near the intended nominal efficiency point.

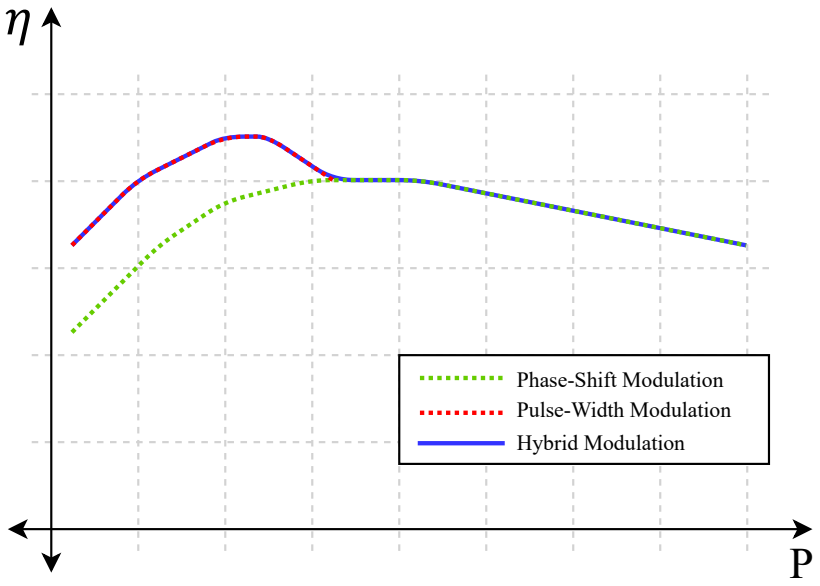


Figure 3.1: Theoretical efficiency curves for PSM, PWM and the Hybrid Modulation

The dynamic implications of this transition must be considered. The converter shifts from a modulation method that generates an alternating waveform at the active bridge output to one that short-circuits the bridge terminals. Such a change can impact the circuit dynamics and component stresses. For this reason, simulation results of the dynamic modulation change are presented in the following section, followed by an analysis of its behaviour under both open-loop operation and closed-loop output voltage control.

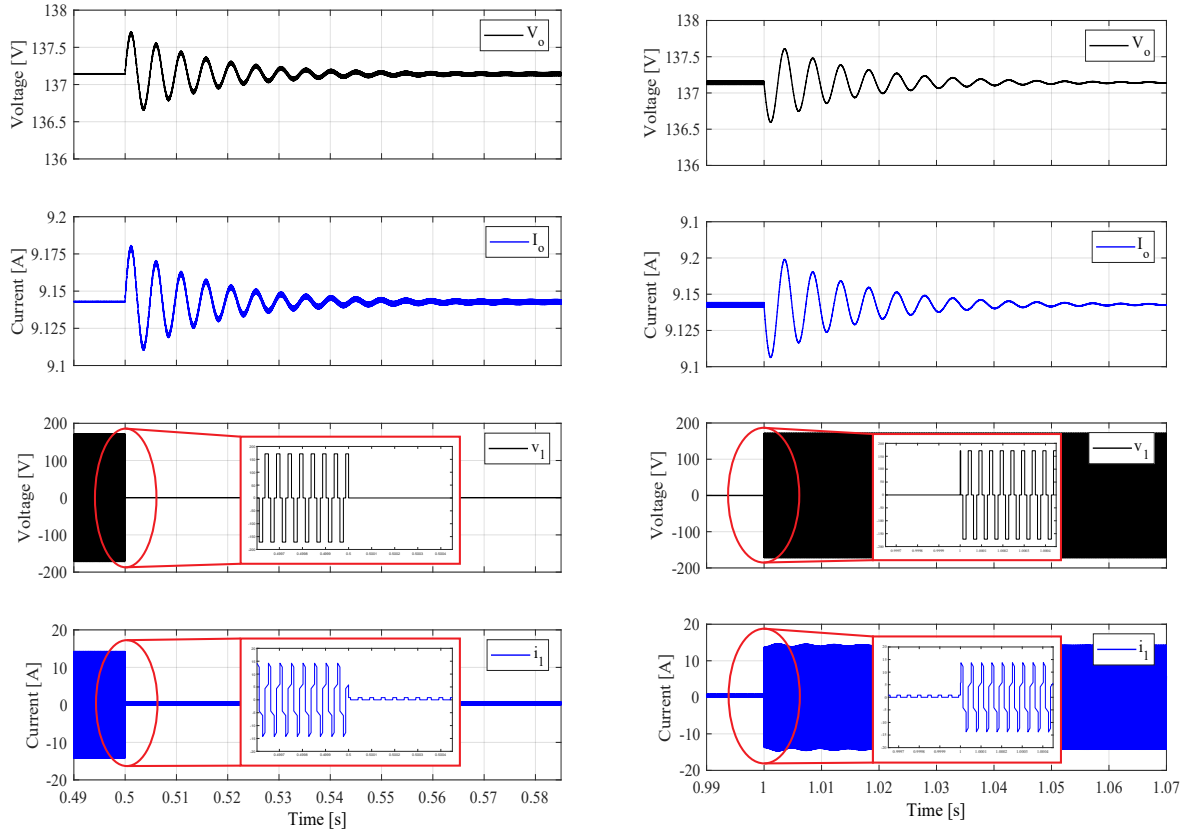
3.0.1 Simulation of Online Modulation Transition

To ensure that the transition between modulation strategies is performed safely while the converter is operating, a simulation is carried out using PLECS. The simulation parameters are the same as the ones used in the previous chapter for efficiency analysis. This first test was conducted in open-loop, that is, with a fixed α in the case of PSM and a fixed d in the case of PWM. To guarantee that the same output voltage was obtained under both modulation schemes, the following relation was applied:

$$d = \frac{2\alpha \cdot n_T}{1 + n_T} \tag{3.1}$$

In this way, the output voltage is set by first selecting a value of α, and then, upon switching to PWM, calculating the corresponding duty cycle d.

Figure 3.2 shows the simulation results for the output voltage and current, as well as the transformer voltage and current, at the instant of modulation change—both from PSM to PWM and from PWM back to PSM.



(a) Transition from PSM to PWM

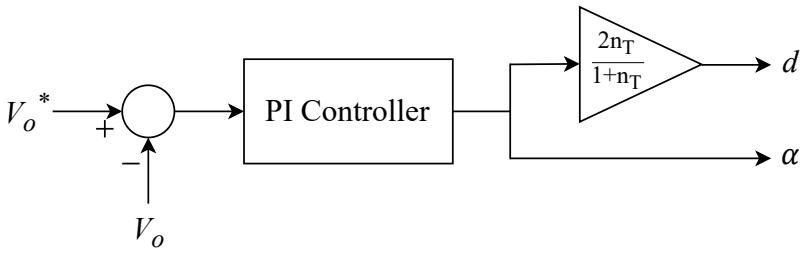
(b) Transition from PWM to PSM

Figure 3.2: Dynamic behaviour of key signals upon modulation transition on Open-Loop simulation

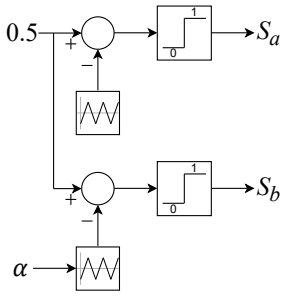
It can be observed that a small transient occurs at the moment of modulation change, which is expected given the significant variations introduced in the circuit's operating conditions. However, the figure shows that the amplitude of the output voltage and current transient is very limited, remaining below 1%. Furthermore, the transient decays rapidly; in the case of the transition from PSM to PWM, it lasts less than 0.1 seconds. On the other hand, for the transformer voltage and current waveforms, a zoom on the signal is required since the transient is even smaller. It can be seen that when switching from PSM to PWM, the transformer voltage immediately drops to zero, while the current—although of very small amplitude—does not vanish completely. This residual current is attributed to circulating currents caused by the magnetizing inductance included in the transformer model.

Based on these observations, it can be concluded that in open-loop operation there are no significant issues associated with the transition between modulation strategies, and that the proposed hybrid modulation approach can be safely implemented.

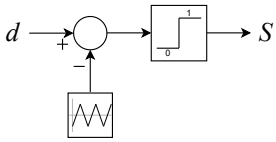
Having confirmed that the transition between modulation strategies within the hybrid approach can be safely executed under open-loop operation, the next step is to analyse the case in which the output voltage is regulated by a simple feedback control scheme. The control architecture is shown in Fig. 3.3. As illustrated, the same controller is employed for both PSM and PWM



(a) Output voltage control scheme



(b) PSM implementation



(c) PWM implementation

Figure 3.3: Control scheme and modulations implementation

operation. The controller processes the output voltage error with respect to a given reference and computes the phase-shift angle α for PSM. This value of α is then passed through a gain factor derived from the relationship expressed in equation 3.1, producing the corresponding duty cycle d required to regulate the output voltage when operating under buck operation. The figure also highlights the implementation of both modulation strategies within the control framework.

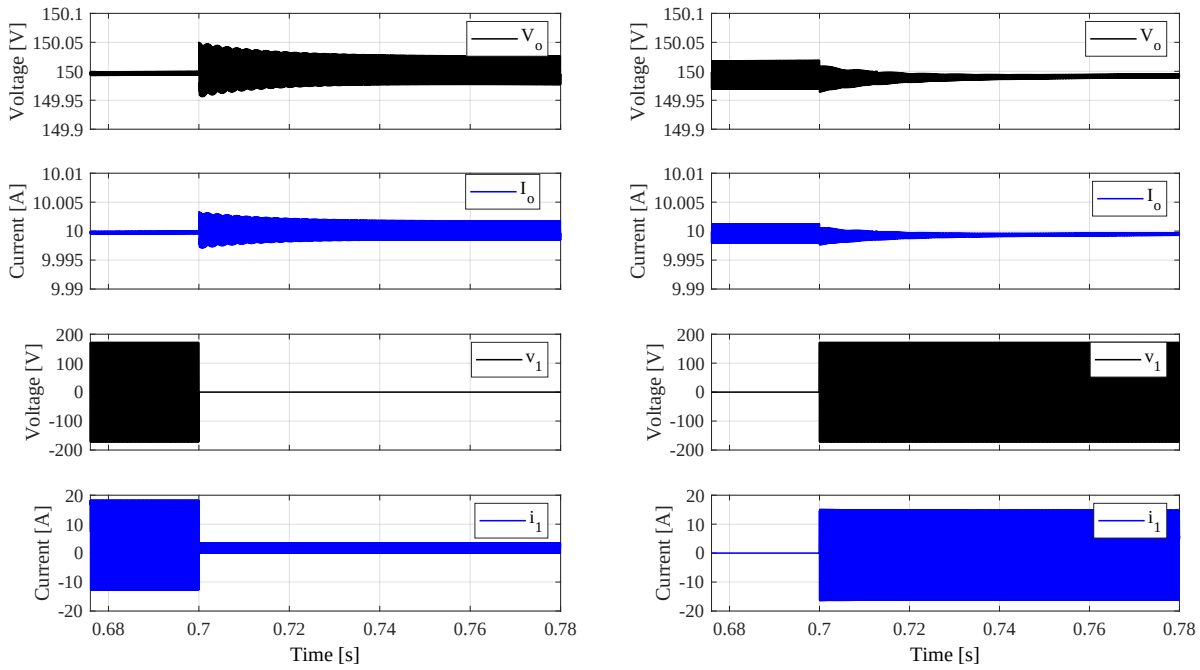
To finalize the comparison of the modulation transition dynamics under both open-loop and closed-loop operation, Fig. 3.4 presents the key operating waveforms previously shown in Fig. 3.2, this time under closed-loop voltage regulation.

It is evident from the waveforms that, with the implementation of a feedback control scheme, the voltage and current ripple during the modulation transition is significantly reduced compared to the open-loop case. Furthermore, it is also evident that BO introduces higher ripple in both the output voltage and current. Nevertheless, the amplitude of this ripple remains sufficiently low to be considered negligible for any practical application of the converter.

Based on these simulation results, it can be concluded that the transition between modulation strategies during converter operation is safe, both under open-loop conditions and when operating with closed-loop control. This demonstrates that the proposed hybrid modulation strategy is feasible and can be effectively applied to the converter in real-world practical applications.

3.1 Chapter Summary

This chapter presents the proposed hybrid modulation strategy aimed at improving the converter's efficiency during low-power operation. The motivation behind this approach is to reconfigure the



(a) Transition from PSM to PWM

(b) Transition from PWM to PSM

Figure 3.4: Dynamic behaviour of key signals upon modulation transition on Closed-Loop simulation

partial power converter so that, under low load conditions, it processes the entire system power. This allows the converter to operate closer to its nominal power point, thereby maintaining high efficiency.

Since the proposed strategy involves switching between two modulation schemes while the converter may be operating, the chapter analyses the dynamic impact of this transition through simulation. First, an open-loop scenario is evaluated, using a fixed α for PSM and a fixed d for PWM. The results show the presence of a small transient during the modulation change; however, its amplitude remains well within acceptable operational limits.

Subsequently, the same transition is studied under a simple feedback control scheme regulating the output voltage of the converter. The results reveal that the transient response during the modulation change is even smaller compared to the open-loop case, ensuring a smooth and stable transition.

Overall, these findings confirm that the hybrid modulation strategy can be safely implemented in both open- and closed-loop operation, demonstrating its practical feasibility for real-world applications.

Chapter 4

Experimental Setup and Performance Evaluation

In the previous chapters, a comprehensive analysis of the converter's behaviour under the two modulation strategies under study was carried out, and a hybrid modulation scheme was proposed. This scheme combines Phase-Shift Modulation (PSM) and Pulse-Width Modulation (PWM) at different operating points to maintain efficiency close to the peak value for which the converter was originally designed.

This chapter presents the experimental validation of the proposed approach. The converter is implemented using pre-assembled half-bridge inverter modules, which are configured to operate in the desired topology. The complete experimental setup is then described, including the instrumentation and the methodology used to implement both modulation strategies.

Following this, the chapter reports the results of the key operating waveforms of the converter under both PSM and PWM, validating the theoretical analysis developed in Chapter 2. The efficiency of the system is evaluated through both simulation and high-precision experimental measurements, and the performance of the hybrid modulation is also demonstrated. Finally, a discussion of the experimental results is presented, highlighting the correlation with theoretical expectations and the implications for practical applications.

4.1 Converter Prototype and Experimental Setup

The experimental prototype used in this work was assembled from half-bridge inverter modules developed at the Advanced Center for Electrical and Electronic Engineering (AC3E). Each module integrates silicon carbide (SiC) MOSFETs as power switches, together with an on-board gate driver that manages their operation. External control is provided via fibre-optic receivers, ensuring galvanic isolation and robust signal transmission.

The modules support two operating modes. In the first mode, one of the fibre-optic inputs enables a dead-time function, while the second input provides the modulation signal; the complementary gate signal required to drive the second MOSFET is then generated automatically by the module. In the second mode, both MOSFETs are driven independently, with each fibre-optic port receiving a dedicated switching signal. For the purposes of this study, the second mode was selected, since Buck operation requires independent control of the MOSFETs and cannot rely on complementary gate signals. Another consideration that was taken when using these pre-designed modules was

Figure 4.1: Experimental implementation of converter

that in the original model, decoupling capacitors are included in parallel to each half-bridge. These had to be removed, since in BO this would have been short-circuited and could have exploded. A detailed description of the module design and operation is provided in Appendix A.

To build the full converter, two of these half-bridge modules were interconnected to form the active full-bridge stage of the inverter. The output of this stage was connected to the primary winding of a high-frequency transformer with a turns ratio of 24:18. The transformer secondary was then connected to a diode bridge rectifier. From there, the rectifier's positive terminal was tied to the inverter's positive bus and subsequently to the output inductor, while the negative terminal was connected to the negative rail, which is shared by the input source, the output capacitor, and the load. This configuration reproduces the full-bridge step-down PPC topology analysed in Chapter 2 and enables the experimental evaluation of both PSM and PWM strategies.

With the prototype converter implemented, the next step is to describe the complete experimental setup used to evaluate the two modulation strategies. The setup (shown in Fig. 4.2) comprises not only the power converter itself, but also the auxiliary circuits, control hardware, measurement equipment, and load interface required to reproduce realistic operating conditions and capture accurate performance data. The experimental arrangement is now presented, providing a comprehensive overview of how the system was configured to validate the theoretical and simulation results presented in Chapter 2.

The experimental setup consists of 8 elements:

- **Workstation PC:** This is the where both modulation strategies are programmed. The control algorithms are first developed in MATLAB/Simulink, where the switching sequences for PSM and PWM are implemented. HMIs are then designed for each modulation strategy using the dSPACE ControlDesk application. Through this interface, the control signals are transmitted to the dSPACE platform, which subsequently delivers the appropriate gate signals to the converter.
- **Interface Board and dSPACE:** The program previously developed on the workstation PC is executed on the dSPACE system, where the gate pulses for the converter's power semiconductors are generated. These pulses are delivered through the analogue output

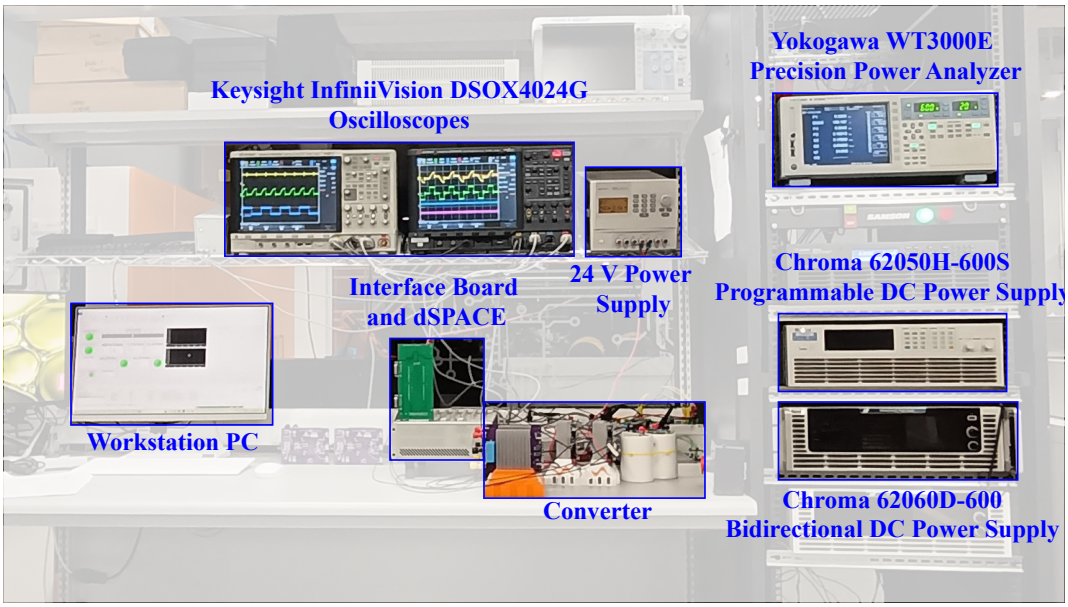


Figure 4.2: Experimental set-up

channels of the dSPACE and subsequently processed by an interface board. The primary function of this board is to convert the electrical gate signals into optical pulses, which are then transmitted via fibre-optic links to the terminals of the half-bridge modules of the converter. The use of this interface is essential, as optical transmission significantly mitigates the electromagnetic noise typically associated with high-frequency gate-drive signals for MOSFETs. It is worth noting that this interface board was designed and built by former colleagues at the POWERLAB of the Department of Electronics at UTFSM.

- **Converter:** The converter prototype was previously described in this section.
- **24 V Power Supply:** This power supply is used to provide the auxiliary power required by the gate drivers of the half-bridge modules.
- **Programmable DC Power Supply:** This DC source provides the input voltage V_{in} of the converter. It is a programmable Chroma 62050H-600S power supply, which allows configuring both the DC voltage supplied and the maximum deliverable current.
- **Bidirectional DC Power Supply:** This Chroma 62060D-600 bidirectional power supply is used as an active load during the experiments. The maximum power and current limits are configured in advance, after which the effective load resistance can be adjusted to vary the consumed power. It is important to note that, when operating in load mode, the supply can emulate different load types such as RC, RL, or purely resistive (R). For all experiments presented in this work, the supply was operated in resistive load mode (R).
- **Oscilloscopes:** Two Keysight InfiniiVision DSOX4024G oscilloscopes are used in the setup. These are connected to differential voltage probes and high resolution current probes. On the first oscilloscope, channels one, two and three are displaying voltages and channel four display current. On oscilloscope two, channels one and three display currents and channels two and four show voltages.

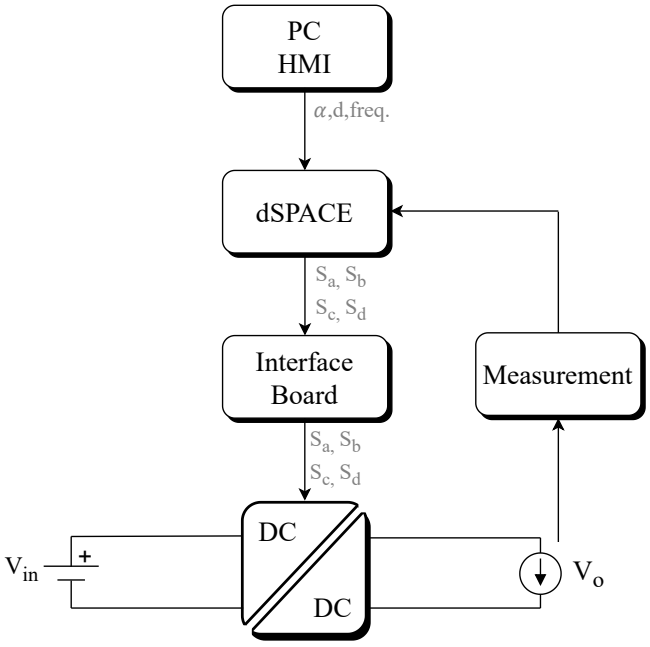


Figure 4.3: Modulation implementation diagram

- **Power Analyser:** A Yokogawa WT3000E precision power analyser is used to calculate the converter's efficiency. This instrument measures input power at the input terminals of the converter and output power at the load. With these measurements it calculates system's efficiency.

With the converter prototype and the complete experimental setup now established, the next step is to detail how the modulation strategies are implemented in practice. This includes the development of the control algorithms in MATLAB/Simulink, their deployment through the dSPACE platform, and the interfacing required to drive the converter hardware. The following sub-section therefore focuses on the implementation process, bridging the gap between the theoretical modulation strategies discussed in Chapter 2 and their experimental realization.

4.1.1 Implementation of Modulations

Once the experimental setup has been fully described, the next step is to explain the implementation of the modulation strategies. Both Phase-Shift Modulation (PSM) and Pulse-Width Modulation (PWM) follow the same general procedure, with the only difference being the program used to generate the switching signals. The process (illustrated in Fig. 4.3) begins with the development of a Simulink model that interfaces with the dSPACE platform. This model is designed to generate pulse trains with a user-defined duty cycle and frequency. The generated signals are then routed to the dSPACE analogue outputs using the corresponding interface blocks.

For the PSM case, two pulse trains are generated with a user-configurable phase shift α between them. Complementary signals are also derived for each pulse train to properly drive the two

MOSFETs within each half-bridge module, since the modules are configured to operate in independent mode.

After the Simulink programs are developed, Human–Machine Interfaces (HMIs) are created in dSPACE ControlDesk. These HMIs serve as the direct interface between the operator and the system, enabling real-time adjustment of the modulation parameters while the converter is operating. In the case of PSM, the HMI allows configuration of the phase shift α and the switching frequency, whereas for PWM it provides control over the duty cycle and frequency.

Once the programs are uploaded to the dSPACE platform, the modulation signals are computed and the corresponding gate pulses for the four semiconductors of the converter's full-bridge stage are generated. These analogue signals are transmitted to the interface board, which, as explained previously, converts them into optical signals. The optical transmission enables the gate driver of the active bridge to receive the signals via fibre optics, effectively mitigating the electromagnetic noise associated with high-frequency switching. The interface board is directly connected to the half-bridge modules, which integrate the MOSFET gate drivers of the full-bridge stage.

With the modulation strategies implemented through the combined use of Simulink, dSPACE, and the interface board, the system is fully prepared for experimental testing. The next section presents the laboratory results, focusing on the converter's operation and efficiency under both PSM and PWM and later efficiency results for the hybrid modulation strategy.

4.2 Steady-State Performance Analysis

This section presents the experimental results obtained from the laboratory tests. The tests were designed to replicate the parameters used in the simulations, as listed in Table 2.2. A series of experiments were conducted at selected fixed output voltage levels, while the load was varied to achieve different operating points of output power. In each case, key operating signals of the converter were recorded, and the system efficiency was measured with high accuracy.

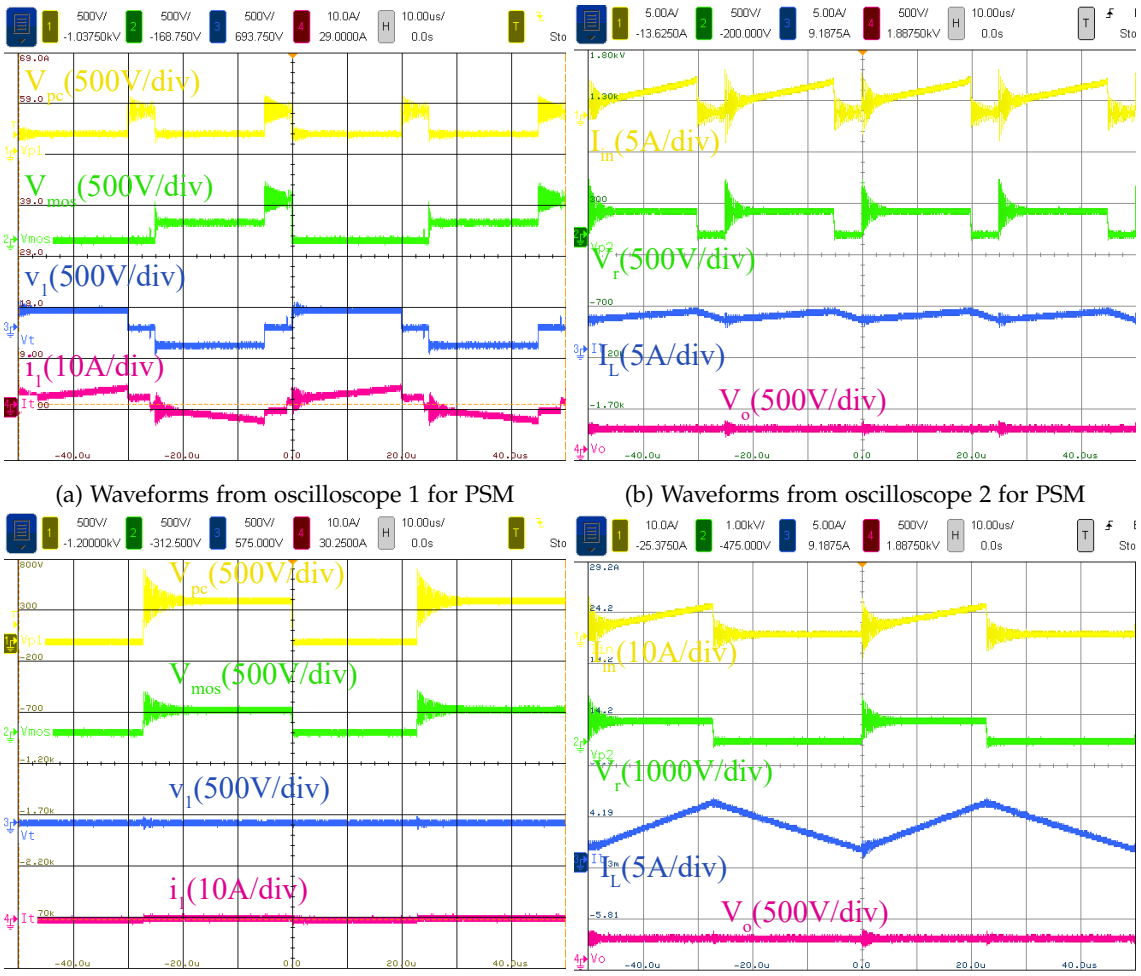
After validating the operation of both modulation strategies and evaluating their efficiency individually, the study also examined the performance of the system when applying the proposed hybrid modulation scheme.

With this framework established, the following subsections present the measured waveforms and efficiency results, providing a direct comparison with the theoretical and simulated analyses discussed in Chapter 2.

4.2.1 Key Operation Signals

Figures 4.4 and 4.5 present oscilloscope screenshots from the laboratory corresponding to a set of experimental tests. These tests were conducted at output voltages of 180 V, 170 V, 150 V, 120 V, and 70 V. The figures shown correspond to the cases of maximum and minimum output voltage operation.

It is important to note that, in these experiments, the maximum output voltage attainable when operating the converter with PSM can be calculated using equation 2.9. Given that the input voltage is $V_{in} = 400V$, the transformer turns ratio is $n_T = 24/18$, and the maximum applicable phase shift is π, the theoretical maximum output voltage is 228 V.



(a) Waveforms from oscilloscope 1 for PSM

(b) Waveforms from oscilloscope 2 for PSM

(c) Waveforms from oscilloscope 1 for PWM

(d) Waveforms from oscilloscope 2 for PWM

Figure 4.4: Key operation signals for both modulations for $V_o = 180V$

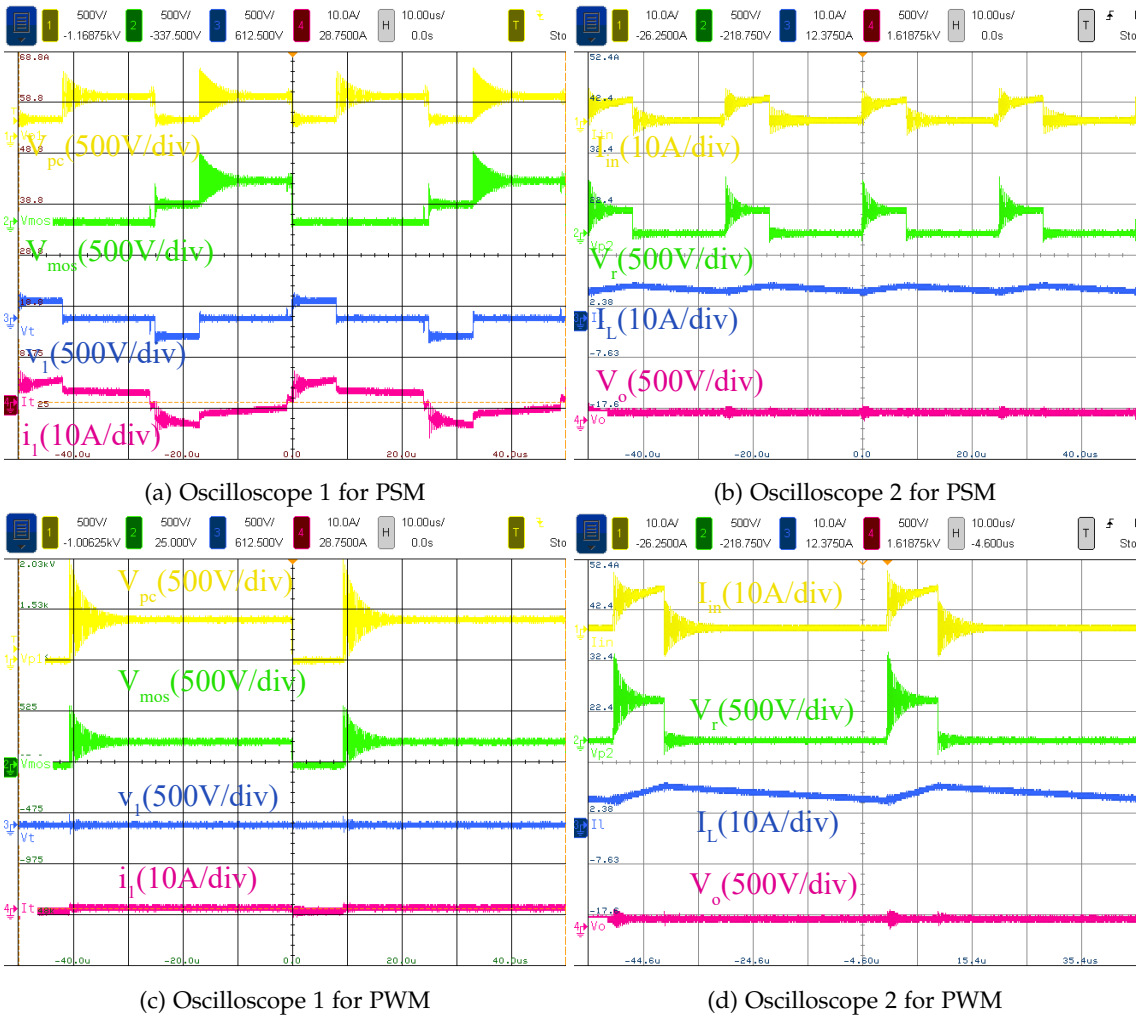
The recorded signals were distributed across two oscilloscopes:

Oscilloscope 1:

- **Channel 1:** Converter voltage at the active bridge V_{pc}.
- **Channel 2:** Voltage across one MOSFET of the active bridge.
- **Channel 3:** Transformer primary voltage v_1.
- **Channel 4:** Transformer primary current i_1.

Oscilloscope 2:

- **Channel 1:** Input current of the converter I_{in}.
- **Channel 2:** Voltage across the diode rectifier bridge V_r
- **Channel 3:** Output current I_o.



(a) Oscilloscope 1 for PSM

(b) Oscilloscope 2 for PSM

(c) Oscilloscope 1 for PWM

(d) Oscilloscope 2 for PWM

Figure 4.5: Key operation signals for both modulations for $V_o = 70V$

- **Channel 4:** Output voltage V_o.

The first case analysed corresponds to an output voltage of 180 V. The captures shown represent an operating point at approximately half of the rated power range, between 550 W and 650 W. The results obtained with PSM are presented first. As predicted by theory, achieving a high output voltage requires a large phase shift between the inverter legs, which can be observed in Fig. 4.4(a). In addition, the measured transformer voltage and current waveforms confirm the expected behaviour, thereby validating both the correct implementation of the modulation strategy and the proper assembly of the converter.

The analysis then turns to the results with PWM. The experimental waveforms closely match the theoretical behaviour discussed in Chapter 2. The voltage at the active bridge—operating as a single switch in this case—exhibits a frequency equal to the switching frequency and a higher amplitude than in the PSM case. Sub-figure (c) shows that both the transformer voltage and current are either null or negligibly small. Finally, Fig. 4.4(d) highlights that the inductor current is higher in amplitude and lower in frequency compared to PSM, further validating the theoretical predictions.

In contrast to the previously analysed cases, Figure 4.5 shows the waveforms recorded during converter operation at an output voltage of 70 V. In this scenario, because the output voltage is significantly lower, the converter must handle a much larger voltage reduction. To satisfy the input–output voltage equations in the ISOP configuration, the converter generates a voltage of $V_{pc} = 330V$. This is clearly observed in sub-figure (a), where both V_{pc} and the voltage across one MOSFET of the active bridge are considerably higher than in the 180 V case. This behaviour is achieved by operating with a reduced phase-shift.

The transformer waveforms further illustrate this effect: within one carrier period, the transformer remains inactive for most of the time, which is consistent with the theoretical expectations. In sub-figure (b), it can also be seen that the output current is much higher than in the previous case due to the lower output voltage, while the operating power point remains approximately the same as in the 180 V experiment.

For the PWM case, the voltage at the active bridge is also higher than in the 180 V test, as the converter must accomplish a greater voltage reduction. Nevertheless, both the transformer voltage and current remain close to zero, as expected from the operating principle of this modulation.

4.2.2 Efficiency Comparison

In the previous subsection, it was confirmed that the converter operates as expected according to theory when applying both modulation strategies. This validates not only the correct implementation of the modulation schemes but also the proper assembly of the converter and the adequacy of the experimental setup. With these foundations in place, the focus now shifts to the core objective of this work: improving the converter's efficiency at low output power through the use of Buck operation, and ultimately, the hybrid modulation strategy.

As previously mentioned, the experiments were carried out at five output voltage levels: 180 V, 170 V, 150 V, 120 V, and 70 V. In each case, the bidirectional DC source, used as an active load, was configured to vary the consumed power by adjusting the effective resistance. The operating range considered in the tests spanned from approximately 300 W to 1200 W. Below 300 W, the converter processes very low currents, approaching discontinuous conduction mode, while above 1200 W, the current demand becomes excessive for both the semiconductor devices and the transformer. It is important to note that the converter was designed to process 600 W in partial-power mode.

The results of these experiments are shown in Figure 4.6. When operating with PWM, the tests reached a maximum of 600 W output power, consistent with the fact that under this modulation, the converter operates as a full-power converter, and 600 W corresponds to its design limit in partial-power operation. The results further indicate that, across all tests, the efficiency of PSM drops at low output power levels, as expected. In this same operating region, Buck operation consistently achieves higher efficiency.

The results presented do not suggest that the partial power converter becomes "inefficient" at low power levels. By design—processing only a fraction of the system's total power—PPCs inherently maintain high efficiency. This is evident in the experimental measurements, where the converter achieves efficiencies above 97% when operating near nominal power, a remarkable performance for most applications in which PPCs are employed. The observed reduction in efficiency at low power does not imply that this topology or configuration becomes unsuitable in that range; in fact, except for the 70 V case, the drop is limited to approximately one percentage point.

Having said that, the proposed modulation strategy clearly enhances the converter's efficiency within the target operating range, in some cases even exceeding the maximum efficiency achieved under PSM. This improvement can be attributed to the fact that, when operating with PWM, the transformer is no longer part of the power-processing path, thereby eliminating its inherent losses. Furthermore, with PWM the switching frequency of the diode bridge is reduced, which further decreases the overall system losses.

These findings validate the research hypothesis and demonstrate the potential benefits of adopting the proposed hybrid modulation strategy.

All efficiency results were obtained using a high-precision Yokogawa WT3000E power analyser. Efficiency was determined by comparing the input power, measured directly at the source, with the output power, measured at the load. Figures 4.7 show the captured waveforms corresponding to the maximum efficiencies achieved in each experiment, providing supporting evidence for the results discussed above.

4.2.3 Hybrid Operation for Efficiency Maximization

Building on the results presented in the previous section, this part introduces the experimental findings for the hybrid modulation strategy. Figure 4.8 illustrates the efficiency curves obtained with this approach.

The results obtained provide clear evidence that the hybrid modulation strategy effectively enables the converter to operate with consistently optimal efficiency. This outcome broadens the potential operating range of the converter, thereby extending its applicability to systems with variable power operating points, such as energy storage system charging interfaces.

Furthermore, the efficiency curve achieved under this strategy closely resembles the theoretical curve presented in Chapter 2 (Fig. 3.1). These experimental findings thus provide strong validation of the research hypothesis established at the beginning of this thesis. The hybrid modulation strategy emerges as a highly compelling alternative to the conventional practice of employing a single modulation scheme. Moreover, it highlights the potential for future research on adaptive modulation strategies aimed at maximizing the utilization of available hardware across diverse applications.

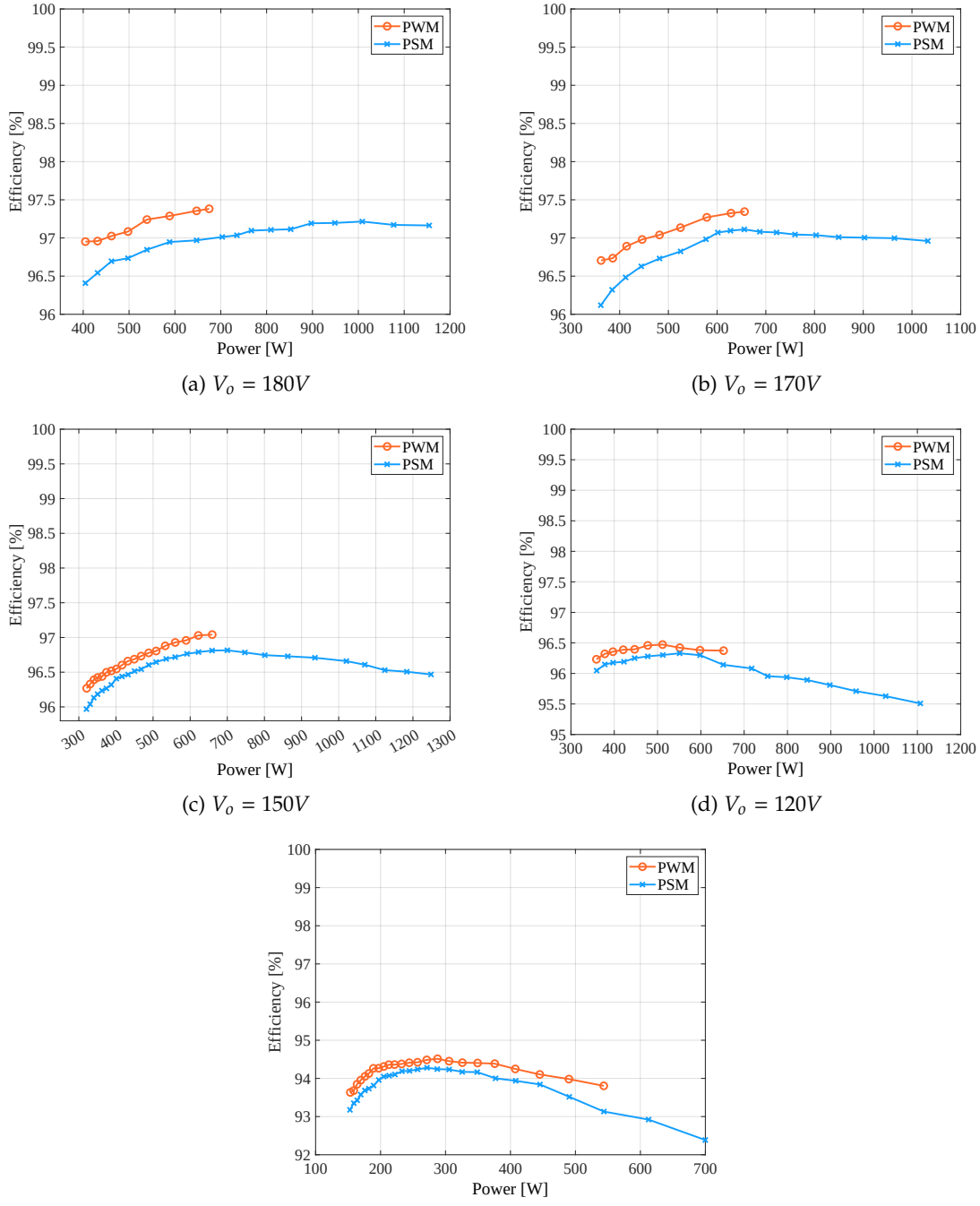
It is important to note that the experimental tests did not include online modulation transitions during converter operation. Instead, each operating point was individually tested using both modulation strategies, and the efficiency curve of the hybrid approach was subsequently reconstructed from these independent results.

4.3 Discussion

Discussion of the obtained results will be divided into three categories: waveform observations, efficiency interpretations, and practical recommendations and limitations.

4.3.1 Waveform observations

The oscilloscope screen captures in Fig. 4.4 and 4.5 provide a direct, time-domain window into the physical mechanisms that ultimately determine converter efficiency. The waveforms reveal how



(a) $V_o = 180V$

(b) $V_o = 170V$

(c) $V_o = 150V$

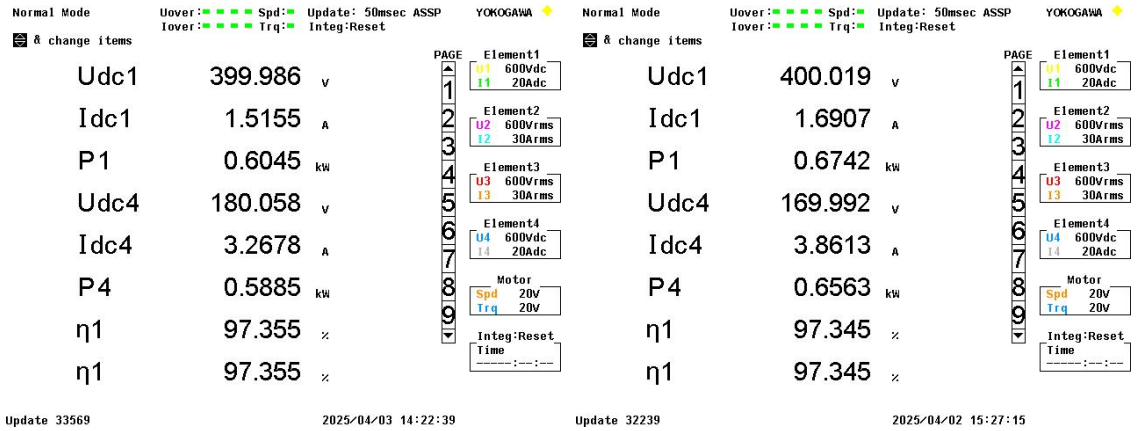
(d) $V_o = 120V$

(e) $V_o = 70V$

Figure 4.6: Experimental efficiency results

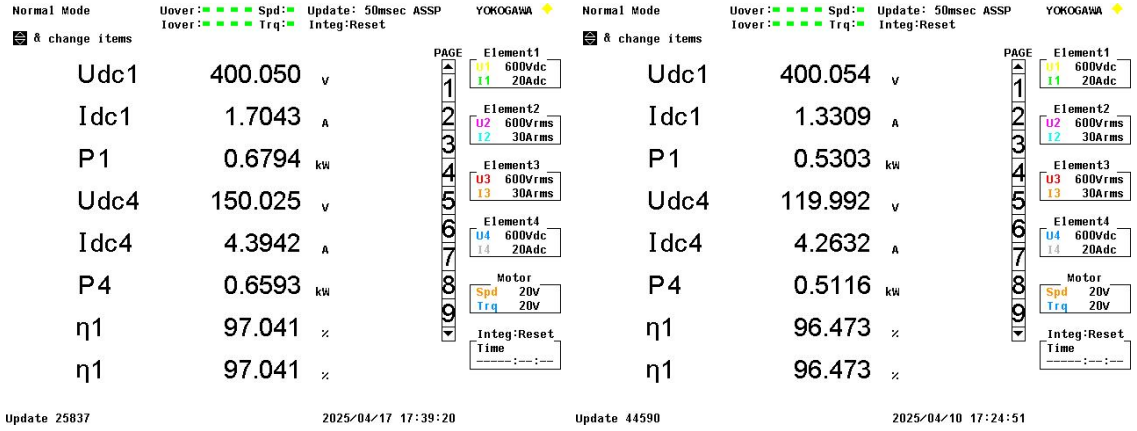
each modulation shapes the power-processing path, and the distribution of voltages and currents across magnetics and semiconductors. Interpreting these traces, therefore, permits to identify the dominant loss contributors for each modulation and to explain the measured efficiency trends observed across the operating range.

A first and decisive difference appears in the transformer excitation. Under PSM the primary



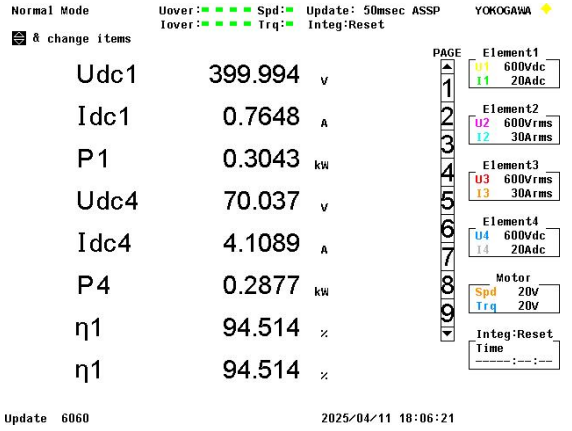
(a) $V_o = 180V$

(b) $V_o = 170V$



(c) $V_o = 150V$

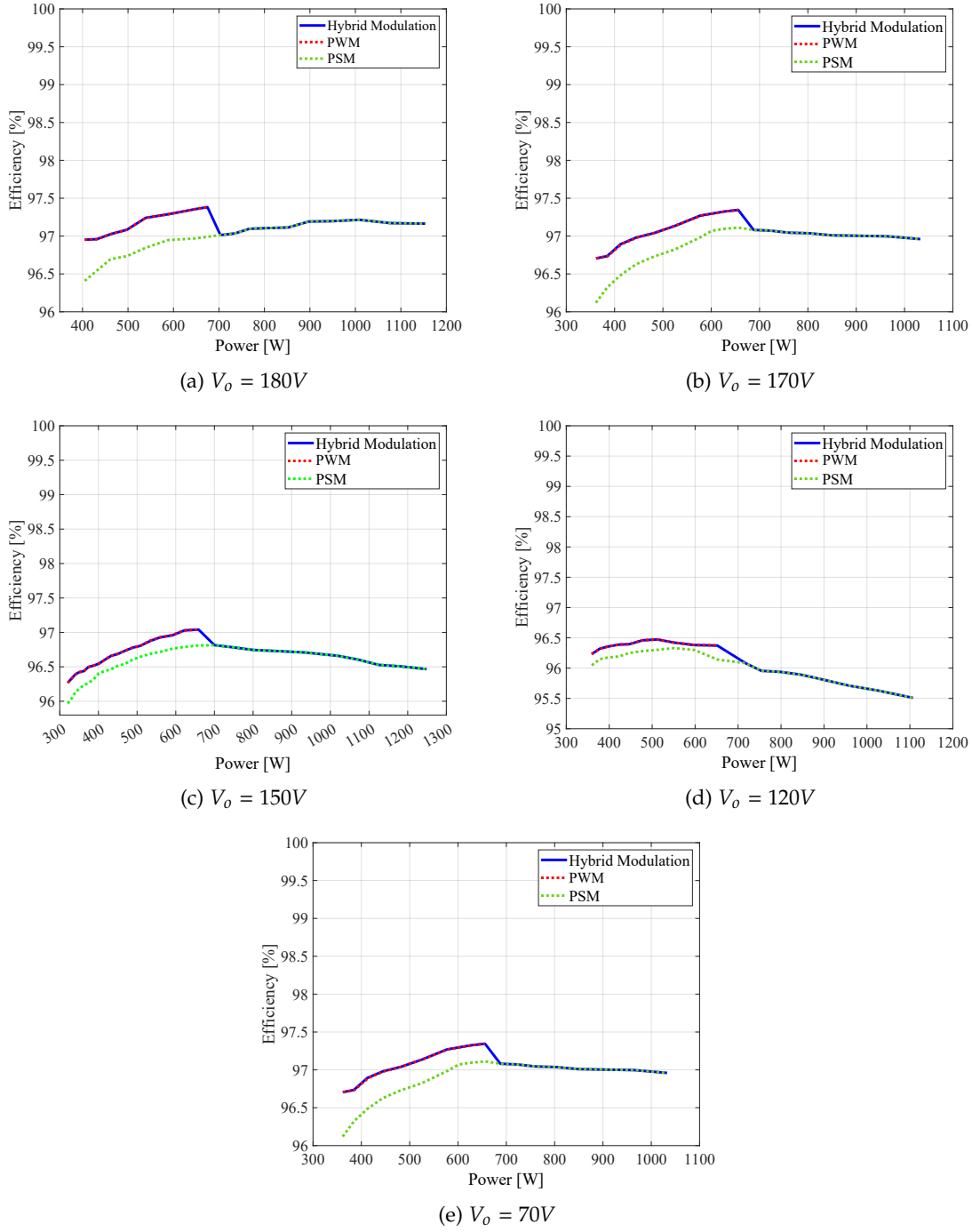
(d) $V_o = 120V$



(e) $V_o = 70V$

Figure 4.7: Maximum efficiency recorded in experiments

is driven by a three-level AC waveform whose effective duty — and therefore the rectified DC level — is controlled by the phase angle α. The measured primary voltage and current traces show this three-level shape with relatively small high-frequency ripple. Because the waveform is closer to sinusoidal (three-level synthesis reduces high-order harmonics), transformer core and copper losses are not as heavily excited as they would be by a square wave; this is one reason PSM



(a) $V_o = 180V$

(b) $V_o = 170V$

(c) $V_o = 150V$

(d) $V_o = 120V$

(e) $V_o = 70V$

Figure 4.8: Efficiency results for hybrid modulation

attains very high efficiency near the design point. By contrast, BO makes the transformer primary voltage essentially zero and the primary current negligible — the transformer is effectively taken out of the power path. The immediate consequence is that transformer core and copper losses are removed from the dominant losses under BO, which is one of the reasons for the efficiency improvement observed at light loads when PWM is used.

Differences in spectral content and ripple location also have important implications for filter design and conduction losses. The recorded inductor currents demonstrate that PWM produces larger amplitude ripple concentrated at the switching frequency (i.e., lower spectral frequency), whereas PSM produces smaller amplitude ripple that appears at approximately twice the switching frequency. Larger, lower-frequency ripple under BO increases the RMS current in the output inductor and in the semiconductor conduction paths, increasing losses unless the filter is re-sized. Conversely, the higher-frequency, lower-amplitude ripple characteristic of PSM is easier to attenuate with smaller passive components and tends to produce lower conduction losses in the filter. Thus, from a waveform standpoint, BO shifts loss contribution from transformer/core to inductor and semiconductor conduction, whereas PSM concentrates losses into transformer excitation and higher-frequency switching.

Taken together, the waveform evidence explains the measured efficiency trade-offs: PSM maximizes efficiency at or near the converter's nominal partial-power design point because it minimizes the fraction of power traversing lossy semiconductor paths; BO improves efficiency at light loads by removing transformer losses and restoring the converter's operating point closer to the design power, but it transfers loss emphasis to conduction and switching in the semiconductors and increases inductor ripple. Practically, this means that any implementation choosing BO must account for larger RMS currents and possibly re-size thermal management and filter components.

4.3.2 Efficiency interpretations

The efficiency measurements presented in Fig. 4.6 provide strong experimental confirmation of the theoretical expectations outlined in Chapter 2, while also highlighting the complementary nature of the two modulation strategies. The first key observation is that PSM achieves its highest peak efficiencies at or near the converter's nominal design point, with recorded values exceeding 97% and in some cases approaching 98%.

However, PSM's performance degrades at light load. The experimental curves demonstrate that efficiency declines slightly when output power drops below nominal, a result of the disproportionate impact of fixed losses. These losses do not scale down with load power. Because PSM deliberately channels only a fraction of total system power through the active conversion stage, when total load power decreases, the absolute power processed becomes very small. As a result, the fixed losses are no longer effectively amortized over significant output power, and efficiency falls. This behaviour is a well-known limitation of PSM and highlights why it cannot maintain high efficiency across the full operating range.

By contrast, PWM shows superior efficiency in the exact operating region where PSM struggles — namely, at reduced load power. Two factors explain this reversal. First, PWM bypasses the high-frequency transformer entirely, thereby eliminating both copper and core losses from the power path. This alone provides a measurable efficiency benefit, especially at lighter loads where transformer magnetizing losses can dominate. Second, PWM forces the converter to process the full system power, effectively re-aligning the operating point with the converter's nominal design utilization. This higher utilization ensures that fixed losses are spread over a greater share of processed power, improving efficiency.

Nevertheless, BO's benefits come with an important operational constraint. Because BO requires the converter to process the full system power, its practical application is limited by the hardware's rated design capacity. In the experimental setup used for this work, this limit was 600 W. Above

this threshold, device ratings, transformer bypass configuration, and thermal constraints would be exceeded, preventing safe or reliable operation. Therefore, while BO offers clear advantages in the low-power regime, it cannot be used as a stand-alone modulation to extend high-power capability. Instead, its role is to complement PSM in hybrid strategies, where the system can dynamically switch between PSM and PWM to maintain peak efficiency across a broader operating range without surpassing hardware limitations.

This interplay between PSM's high efficiency near nominal load and PWM's superior performance at reduced load forms the foundation for the hybrid modulation strategy introduced in this thesis. The experimental efficiency curves clearly illustrate how each modulation addresses the other's weaknesses, confirming the feasibility and practical value of combining them into a unified control approach.

4.3.3 Practical recommendations and limitations

The experimental findings lead to several practical recommendations for applying the proposed modulation strategies. First, hybrid modulation should be prioritized in systems with a wide and variable operating range, such as PV arrays or battery storage interfaces. In these applications, the ability to switch between PSM and PWM provides a net efficiency improvement by aligning the converter's operating mode with the prevailing load conditions.

Second, the use of PWM requires conservative engagement limits. Because BO forces the converter to process the full system power, it is essential to implement safeguards such as current and thermal headroom checks to prevent operation under unsafe conditions. Similarly, transition strategies must be carefully tuned. Performing transitions near current zero-crossings, or using short synchronization intervals with closed-loop control, minimizes switching transients and mitigates magnetizing effects.

Finally, sustained PWM operation alters the ripple spectrum, increasing both amplitude and lowering the dominant frequency. If PWM is expected to be used extensively, redesign of the magnetic components and output filter may be required to ensure stable and efficient operation.

4.4 Chapter Summary

This chapter presented the experimental validation of the converter and modulation strategies introduced earlier in the thesis. A prototype was implemented using SiC half-bridge modules, a high-frequency transformer, and a rectifier, with a complete laboratory setup including precision instrumentation for waveform capture and efficiency measurement. Both PSM and PWM were programmed and controlled via a dSPACE platform, ensuring accurate replication of the theoretical modulation strategies.

The experimental waveforms confirmed the expected converter behaviour under each modulation. Under PSM, the transformer was actively excited, showing the anticipated three-level AC waveform with small high-frequency ripple, while BO effectively bypassed the transformer, leaving its voltage and current negligible. The inductor currents also differed: PSM produced smaller, higher-frequency ripple, while BO resulted in larger, lower-frequency ripple. These results demonstrated how each modulation distributes losses differently across the transformer, inductor, and semiconductors.

Efficiency measurements provided further insight into these differences. PSM achieved very high efficiency near nominal processed power, reaching close to 98%. However, PSM efficiency declined at lighter loads because fixed losses became dominant. In contrast, PWM outperformed PSM at low power by eliminating transformer losses and increasing utilization of the semiconductors, though it was constrained by the converter's 600 W design limit.

Finally, the chapter validated the hybrid modulation strategy, combining the strengths of both approaches. Experimental results showed that hybrid modulation maintains near-optimal efficiency across a wide operating range, closely matching the theoretical predictions. This outcome confirms the validity of the initial hypothesis and highlights hybrid modulation as a promising approach for applications with variable operating conditions, while also suggesting opportunities for further research into adaptive modulation strategies.

Chapter 5

Conclusions

This thesis presented the design, analysis, and validation of a novel hybrid modulation strategy aimed at improving the efficiency and operational flexibility of a full-bridge-based step-down partial power converter (PPC). The research was motivated by the inherent efficiency degradation that conventional phase-shift modulation (PSM) experiences when operating far from its nominal power point, particularly under light-load conditions. By introducing an alternative modulation scheme and combining it with PSM in a complementary manner, this work proposes an approach that expands the converter's effective operating range while maintaining high efficiency.

The first stage of the work consisted of an extensive review of partial power processing concepts and the state of the art of modulation strategies applied to different converter topologies. This review revealed that most of the advances in PPC modulation have focused on dual active bridge (DAB) architectures, where several PSM-derived strategies have been developed to enhance performance. In contrast, modulation approaches for full-bridge-based PPCs remain limited almost exclusively to single phase-shift (SPS). This gap represented an opportunity to contribute new knowledge by exploring modulation alternatives for this particular topology.

Building on this foundation, the thesis proposed an alternative buck operation (BO) scheme, characterized by the synchronous commutation of all four active switches of the full bridge. This effectively reconfigures the converter from partial power processing to full power processing mode, bypassing the transformer and operating like a conventional buck converter. While this may appear contrary to the philosophy of partial power processing, this mode becomes advantageous under low-power operation, where conventional PSM exhibits poor utilization and reduced efficiency.

The subsequent stage introduced a hybrid modulation strategy that dynamically combines PSM and PWM. The converter operates under PSM at nominal or high power levels, ensuring low processed power and high efficiency, while switching to PWM at low power levels to restore efficient operation closer to the nominal design point. This approach allows the converter to maintain high efficiency over a broader range of output power compared to what is achievable with PSM alone. The theoretical analysis demonstrated the complementary nature of both modulations and their potential to overcome the limitations of conventional operation.

The dynamic behaviour of this hybrid strategy was evaluated through simulations, focusing on the transition between modulation modes during operation. Results showed that the transition generates only a small and short-lived transient response, well within acceptable limits for stable operation. This confirmed that the strategy is not only theoretically sound but also dynamically feasible for practical implementation.

Finally, experimental validation was carried out using a laboratory prototype of a step-down full-bridge PPC. Efficiency measurements across different operating points confirmed the simulation results: PWM outperformed PSM at low power levels, while PSM remained superior near the nominal design point. The hybrid strategy successfully combined both behaviours, resulting in consistently high efficiency across the entire tested range. This demonstrates that the proposed hybrid modulation enables better hardware utilization without any physical modification to the converter, relying solely on a change in the modulation of the active switches.

In summary, this thesis contributes a new and effective modulation strategy for full-bridge-based partial power converters. By combining two complementary operating modes, it addresses a key limitation of conventional modulation approaches and enhances the performance of PPCs under varying load conditions. These results reinforce the potential of modulation strategies as powerful tools to improve converter operation without increasing system complexity or cost.

Further work

- To expand the hybrid modulation approach to other full-bridge-based PPC configurations, such as IPOS for step-up operation.
- To apply advanced adaptative control strategies to automate the modulation strategy switching logic.
- To develop a more detailed loss model to optimize the modulation strategy not only for efficiency but also for thermal management and lifetime extension.
- To study the behaviour of the hybrid-modulated PPC under real PV profiles (irradiance variability), dynamic charging loads, or grid support conditions.

Appendix A

Half-bridge inverter experimental module technical report

Inversor de medio puente modular

Polidoro F. Canales

09 de noviembre de 2023

1. Resumen

El diseño corresponde a un inversor de medio puente con MOSFET SiC; esta posee dos receptores de fibra óptica para señales de control externas, su funcionamiento dependerá de cuál de los dos modos de operación disponibles en la PCB se seleccione (detallado en la sección **3.2**). Uno de los modos habilita la función de tiempo muerto y utiliza uno de los receptores de fibra óptica como señal principal para generar la complementaria y el otro receptor como señal de habilitación. En el otro modo se deshabilita el tiempo muerto y permite utilizar las señales de los receptores independientemente una de la otra.

2. Descripción general

El diseño consiste en un inversor medio puente de MOSFET SiC de dimensión estándar para montar en un rack 3U (**100mm x 130mm**); este puede funcionar de dos maneras; en una de ellas es posible utilizar una señal de entrada para controlar los semiconductores de manera complementaria y con tiempo muerto regulable directamente en la placa dependiendo del valor de una resistencia, y el otro modo de operación permite controlar las conmutaciones del MOSFET superior y MOSFET inferior de manera completamente independiente y sin tiempo muerto de por medio; la frecuencia de conmutación del inversor es de **100kHz**.

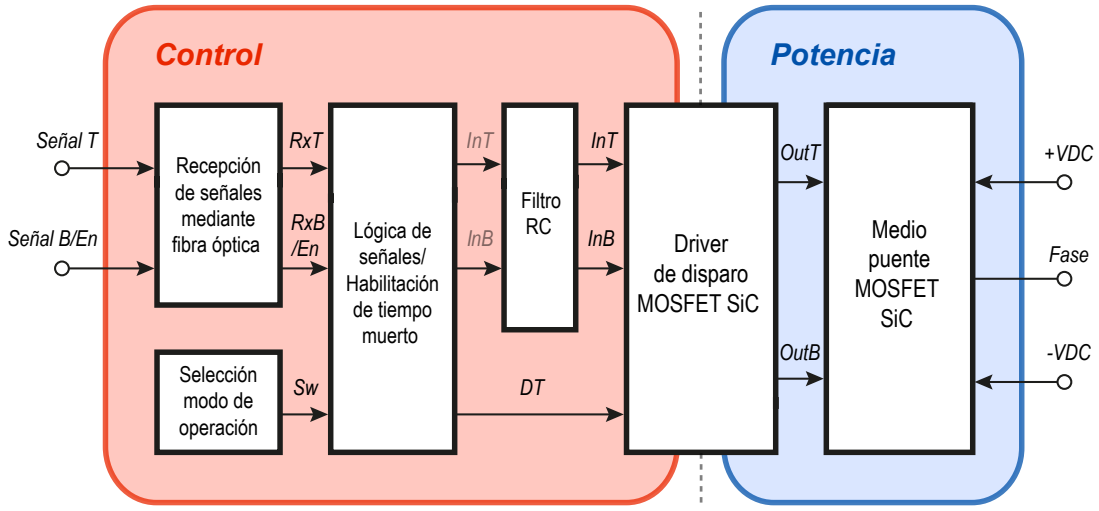


Figura 1: Diagrama general del inversor.

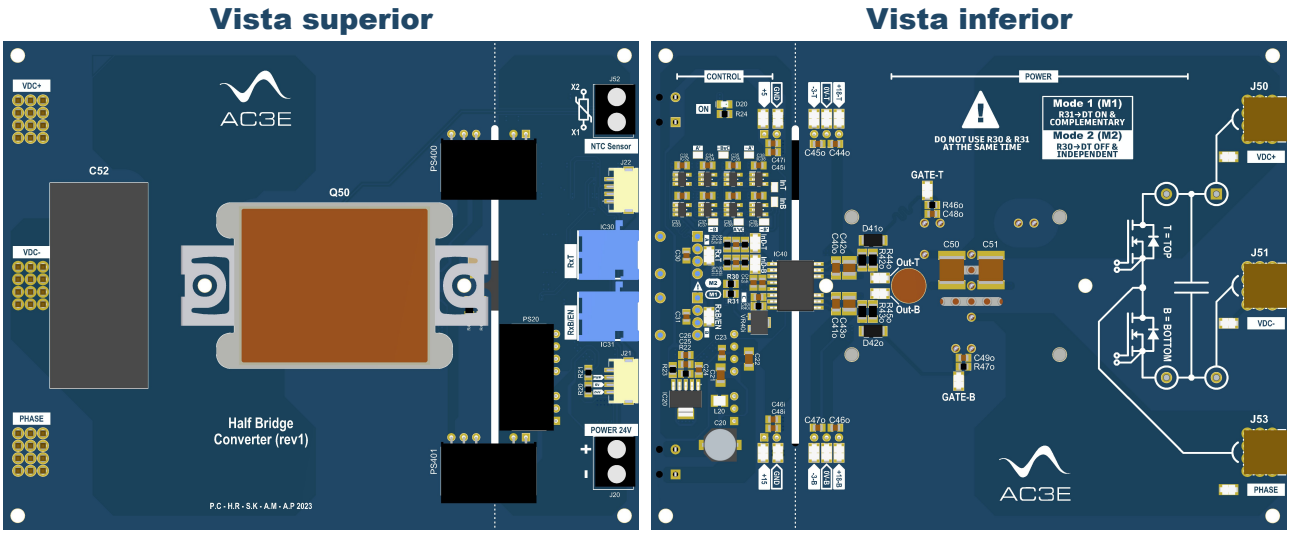


Figura 2: Vista general del inversor.

En la Fig.1 se presenta un diagrama general de las etapas que posee el inversor. Las señales 'T' y 'B/En' corresponden a los pulsos de luz externos proporcionados por el controlador; estos luego de ser transformados a señal eléctrica por los receptores de fibra óptica llegan a la etapa de lógica, etapa a la cuál también llega el estado de la señal 'Sw' que se encuentra directamente en la placa.

Antes de que la señal de disparo para los semiconductores llegue al driver optoacoplador pasa por un filtro pasabajos (opcional); luego de esto el driver se encarga de generar las señales que van directamente a la compuerta de los MOSFET.

La placa debe ser alimentada con **24V**, sin embargo la parte de control funciona con **5V** para lógica interna y con **15V** para alimentar las fuentes aisladas de los disparos; estas fuentes asimétricas proporcionan voltajes de **-3V/18V** para el driver.

Con respecto a la etapa de potencia, el mediopuente de MOSFET SiC conduce **25A** nominales y un voltaje de **1200V**.

En la Fig.2 se presenta una vista 3D general de la tarjeta con la disposición de los componentes montados a excepción del disipador térmico debido a que sus dimensiones pueden variatr dependiendo de la cantidad de calor que se necesite disipar.

3. Etapas

A continuación se muestran en detalle los circuitos con sus respectivos esquemáticos que componen la parte de control y la parte de potencia de la tarjeta.

3.1. Alimentación

La placa se alimenta de una fuente DC externa de **24V** y a través de un DC/DC (**SPBW06F-15**) se generan **15V** como se muestra en la Fig.3. Los capacitores $C21$ y $C22$ son de desacople y es opcional soldarlos a la placa en el caso de que la fuente externa posea bajo ruido. También se encuentra disponible un punto de prueba para medir los **15V**. Es importante mencionar que la tierra de la alimentación externa se encuentra aislada de la tierra de la etapa de control.

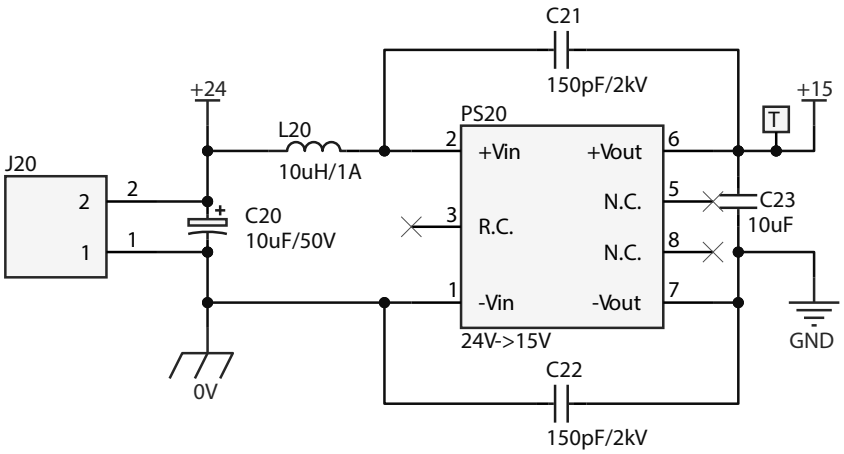


Figura 3: Esquemático alimentación principal a 15V.

En la Fig.4 se encuentra el circuito posterior a la etapa de entrada, en donde obtienen **5V** a partir de los **15V** de la etapa anterior mediante el uso de un regulador de voltaje (**TPS73801DCQR**). El LED $D20$ cumple solamente la función de indicar si el circuito de **5V** está siendo energizado; en caso de desear corroborar el valor puede utilizarse el punto de prueba disponible.

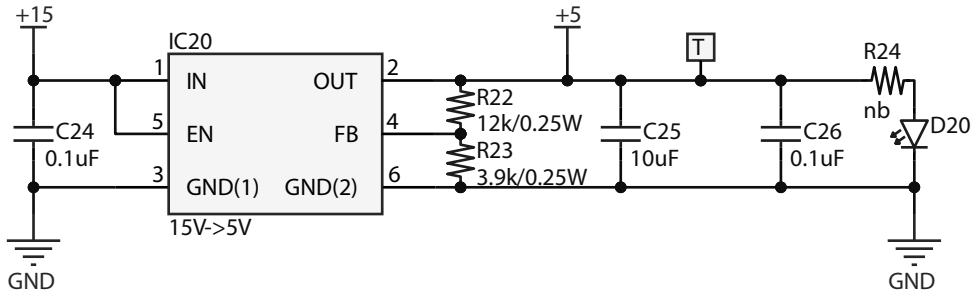


Figura 4: Esquemático regulador de 15V a 5V.

Para la etapa del circuito encargada de los disparos de los semiconductores se utilizan fuentes DC/DC (**QA01C-18**) que a partir de los **15V** suministrados se generan **18V** para la activación de los switches y **-3V** para la desactivación. En la Fig.5 se muestra el esquemático del circuito.

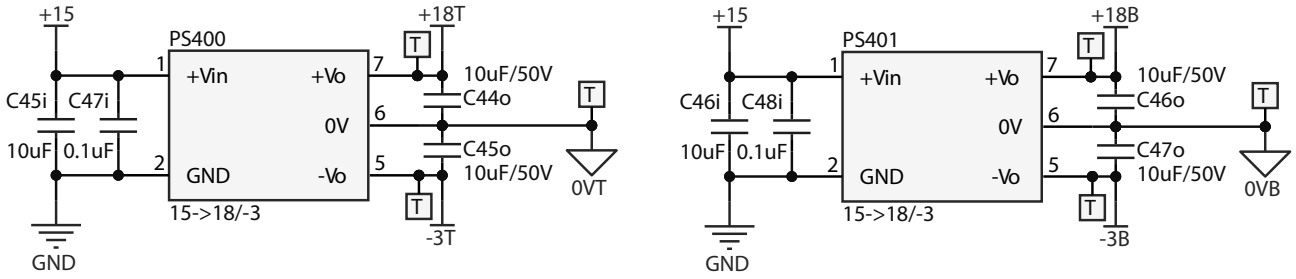


Figura 5: Esquemático alimentación asimétrica para disparos.

Se encuentran disponibles puntos de prueba para todos los voltajes con la función de corroborar si efectivamente se están generando los voltajes deseados. Es importante destacar también que las fuentes asimétricas utilizadas para los disparos son aisladas y la tierra de la etapa de control se encuentra asimismo aislada de la etapa de potencia.

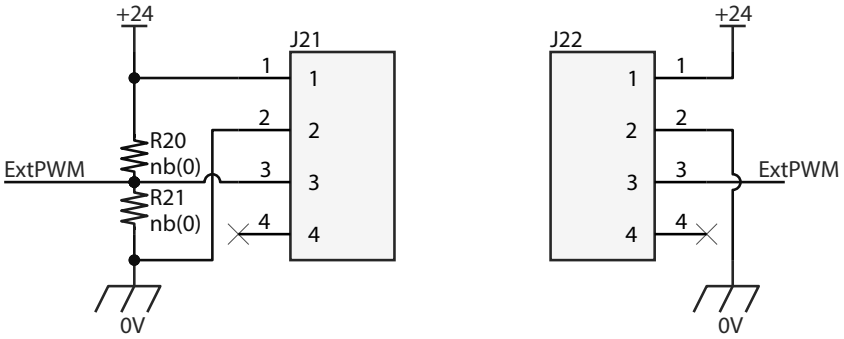


Figura 6: Esquemático circuito ventilador.

Es posible utilizar un ventilador si se desea; se encuentran dos conectores disponibles en la placa, uno de estos permite conectar un ventilador que opere a una tensión de **24V** nominales. Directamente en la placa las resistencias $R20$ y $R21$ que se presentan en la Fig.6 permiten deshabilitar alguna señal de PWM para el caso que no se desee controlar la velocidad de giro de las aspas; en el caso contrario no se debe soldar ninguna resistencia del circuito para permitir el control mediante una señal PWM externa.

El conector $J21$ es el correspondiente al ventilador, y el $J22$ se debe utilizar para controlar el ventilador mediante un MCU externo. En caso de no ser necesario el ventilador no se debe soldar ninguno de los componentes del circuito presentado en la figura.

3.2. Lógica

Para cumplir con los dos modos de operación del inversor mencionados anteriormente se utiliza una etapa de lógica de señales que además de generar las condiciones deseadas posee el mismo retardo para cada uno de los caminos posibles que tomará la señal.

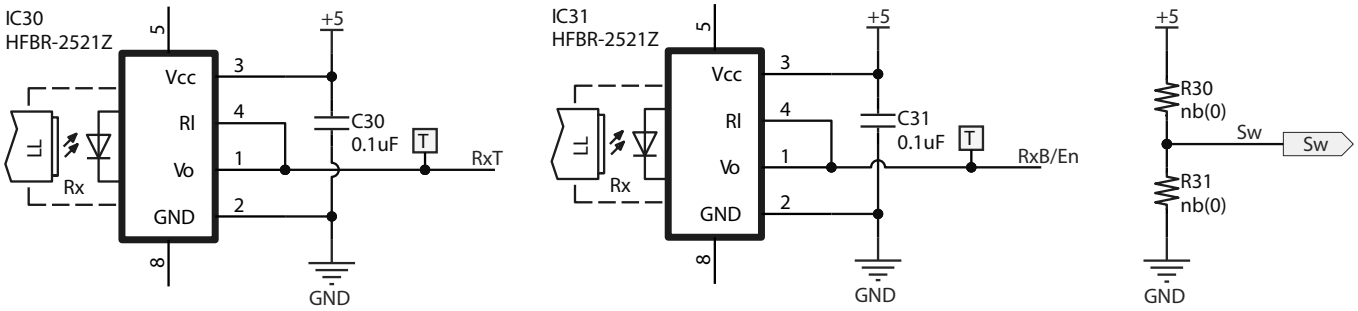


Figura 7: Esquemático recepción señales y modo funcionamiento.

Inicialmente se necesitan dos señales externas que se reciben mediante fibra óptica y una tercera señal que indica el modo de operación a utilizar; esta última se selecciona directamente en la placa mediante el uso de las resistencias $R30$ y $R31$; estas no tienen un valor resistivo, por lo que solo permitirán entregar un valor de **5V** o **GND** al resto del circuito lógico, no deben ser puestas ambas al mismo tiempo. Es importante mencionar que las señales recibidas por fibra óptica al ser transformadas a eléctricas son negadas. La condición que cumplen las resistencias $R30$ y $R31$ es la siguiente:

- Si $R30$ se encuentra soldada, el inversor utilizará las señales recibidas mediante fibra óptica para realizar las conmutaciones de los MOSFETs de forma independiente y sin tiempo muerto de por medio.
- Si $R31$ se encuentra soldada, el inversor utilizará la señal recibida por $IC31$ como una habilitación e $IC30$ para conmutar el MOSFET superior y generará la complementaria de esta para conmutar el MOSFET inferior con tiempo muerto de por medio. Para este modo si no está habilitada la señal de $IC31$ los dos MOSFET se encontrarán como un interruptor abierto.

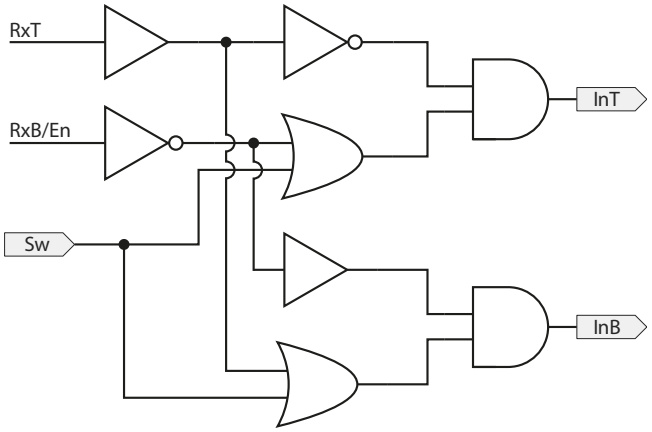


Figura 8: Esquemático condiciones lógicas.

La Fig.8 esquematiza el circuito de lógica inmerso dentro del inversor; la señal pasa por buffers (**SN74LVC1G17DBVR**), compuertas NOT con schmitt trigger (**SN74LVC1G14DBVR**), compuertas OR (**SN74LVC1G32DBVR**) y compuertas AND (**SN74LVC1G08DBVR**). Finalmente InT e InB son las que se generan para el disparo del MOSFET superior e inferior respectivamente previo al driver.

El estado de la señal 'Sw' se mantendrá sin variar debido a que para cambiarlo es necesario manipular el hardware, por lo que el comportamiento de las señales de entrada luego de pasar por el circuito lógico será de una determinada forma dependiendo de esto; en la Fig.9 y la Fig.10 se muestra el comportamiento de la señal en los casos en que 'Sw' esté en un estado alto o bajo respectivamente.

Para el caso de la Fig.9, cuando la señal de los receptores de fibra óptica se encuentra en alto se traduce como ausencia de luz, por consiguiente la señal que se tendrá en la salida de las condiciones lógicas ante esa entrada generará un estado bajo para enviar la instrucción de desactivar el switch al driver. En el caso del otro modo de operación del inversor, cuando la señal del receptor 'RxB/En' se encuentra en alto, ambas salidas del circuito lógico se encontrarán en bajo ya que estarán deshabilitadas, y si esta señal se encuentra en bajo, entonces el circuito lógico generará en la salida la señal del receptor 'RxT' negada y su complementaria.

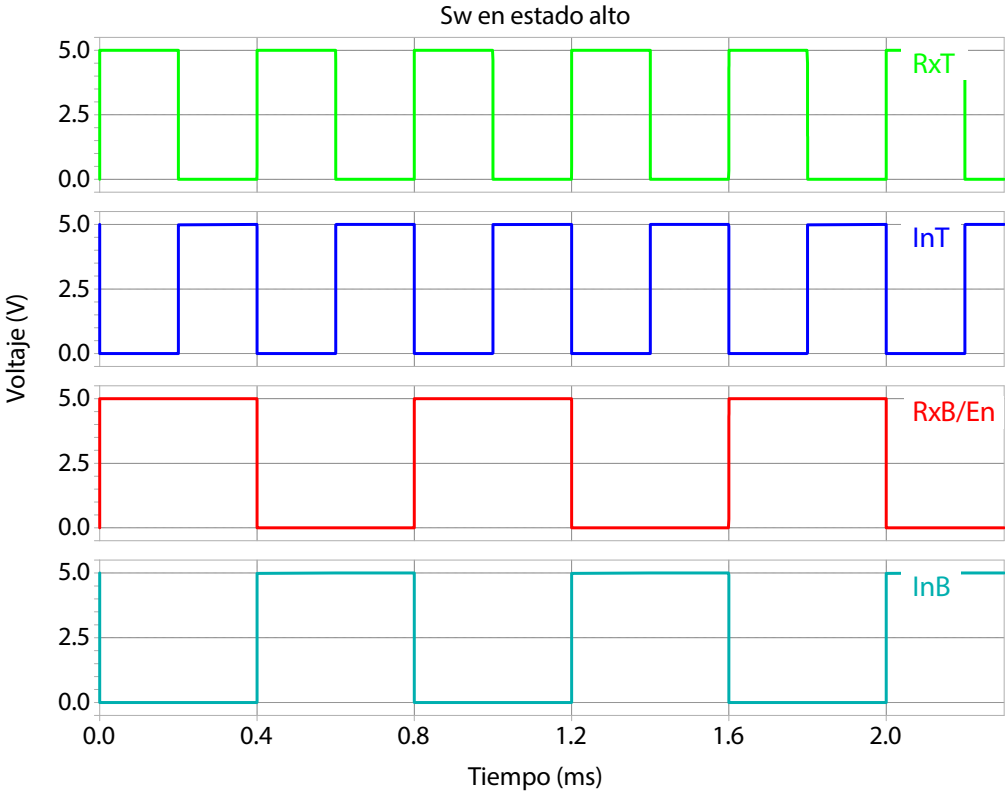


Figura 9: Gráfica de señales con Sw en estado alto.

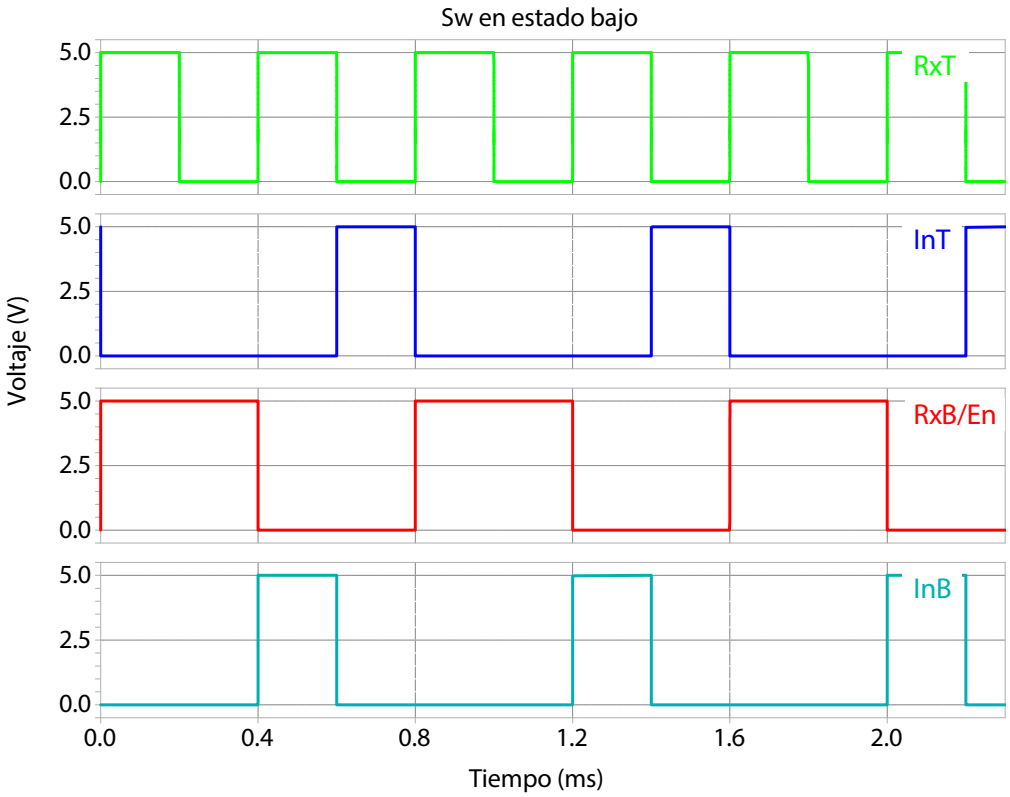


Figura 10: Gráfica de señales con Sw en estado bajo.

3.3. Driver

El driver utilizado (**UCC21540ADWKR**) posee ciertas funcionalidades de las que se sacó provecho en el diseño:

- Tiempo muerto (DT) regulable directamente en la placa dependiendo del valor de $R40i$ o del potenciómetro $VR40i$ y del modo de funcionamiento. La relación es $DT = 10 \cdot R40i$, donde DT está en **ns** y $R40i$ en **k**Ω.
- Las señales de salida del driver pueden utilizarse de manera completamente independiente permitiendo que se sobrepongan, esto corresponde a uno de los modos de operación.
- Posee un tiempo de retardo de unos **5ns** entre la señal de entrada y señal de salida por lo que es lo suficientemente rápido como para conmutar a una frecuencia de **100kHz**.

En cuanto al esquemático presentado en la Fig.11, las señales InT e InB es posible filtrarlas mediante $R42i$ y $R44i$ y mediante $R41i$ y $R43i$ respectivamente; en el caso de no desear pasar por el filtro se deben utilizar resistencias de **0**Ω para $R42i$ y $R41i$ y los demas componentes del filtro se deben dejar sin soldar. Todas las señales de la etapa es posible monitorearlas mediante los puntos de prueba.

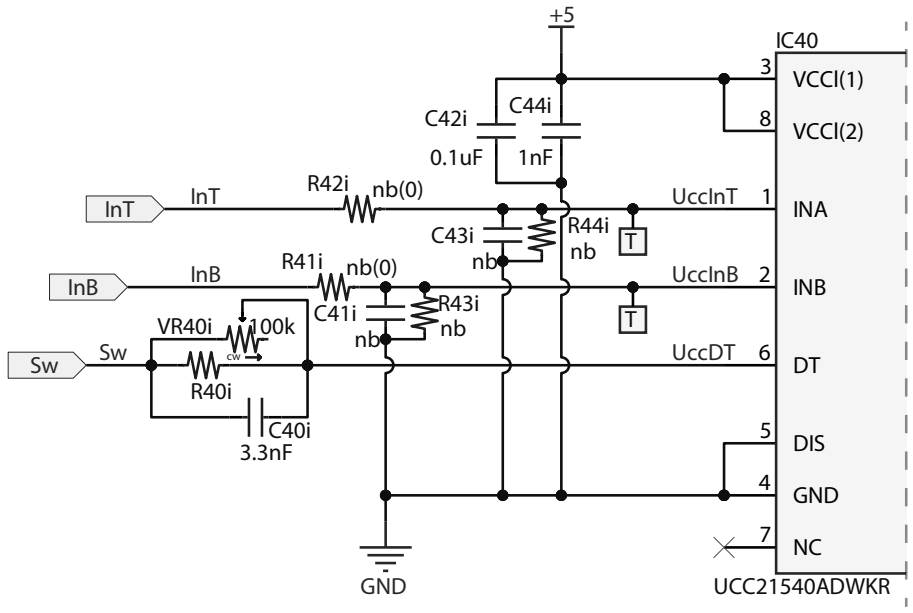


Figura 11: Esquemático circuito de entrada de driver optoacoplador.

A la salida del driver se encuentra el circuito correspondiente a la Fig.12. $D40o$, $R40o$ y $R41o$ componen un circuito de bootstrapping que si no se desea utilizar se debe dejar sin soldar.

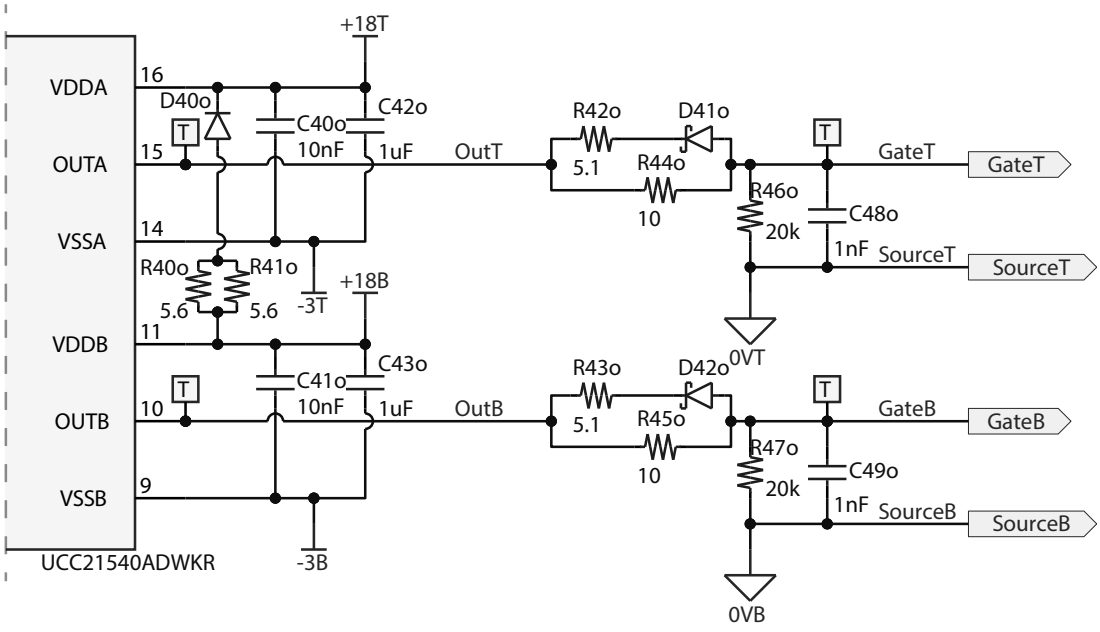


Figura 12: Esquemático circuito de salida de driver optoacoplador.

$R46o$ y $R47o$ son resistencias de pull-down que ayudan a evitar que las corrientes circulantes en la compuerta del semiconductor produzcan algún encendido fantasma, y los capacitores $C48o$ y $C49o$ se encuentran disponibles para modificar la dinámica del apagado y encendido de los MOSFET debido al capacitor Cgs propio de estos.

Todas las señales a la salida del driver se encuentran aisladas de las señales de entrada y a su vez también las que se generan para controlar el semiconductor superior se encuentran aisladas de las que se generan para la activación y desactivación del MOSFET inferior para evitar el traspaso de ruidos y el eventual acoplamiento de alguna señal.

3.4. Potencia

El módulo (**FF33MR12W1M1HP_B11**) que contiene los MOSFET SiC posee la disposición que se muestra en la Fig.13; $C50$ y $C51$ corresponden a capacitores de desacople de la fuente de alto voltaje, y $J50$, $J51$ y $J53$ corresponden a conectores de potencia.

El módulo posee también internamente un sensor NTC de temperatura, cuya señal se ha dejado disponible mediante el conector $J52$ en caso que se desee utilizar con un microcontrolador externo.

El módulo de MOSFET SiC permite operar a una corriente nominal de **25A** y un voltaje de **1200V**

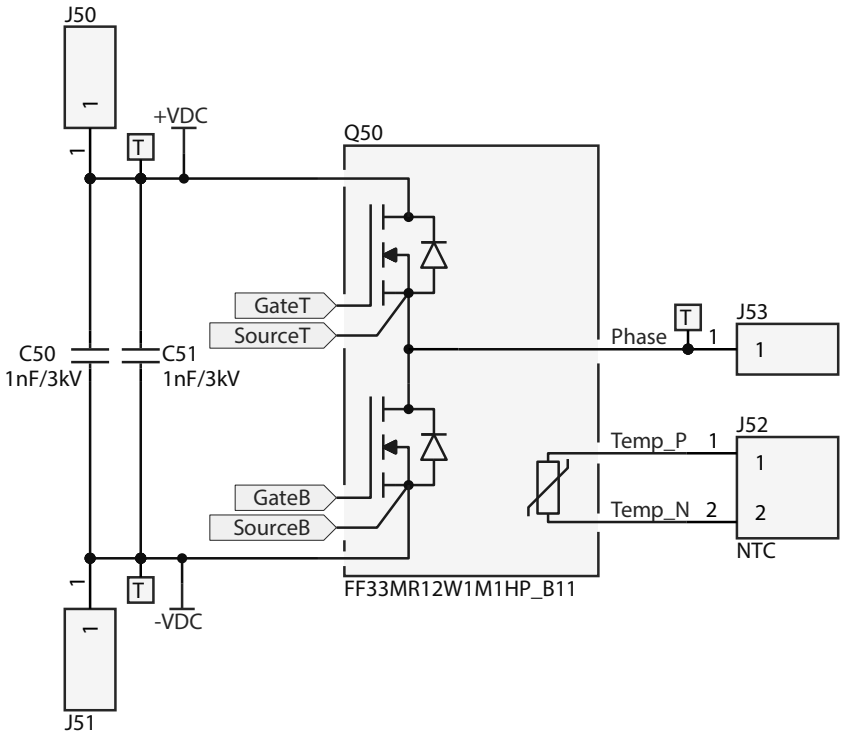


Figura 13: Módulo SiC.

4. Disposición de componentes

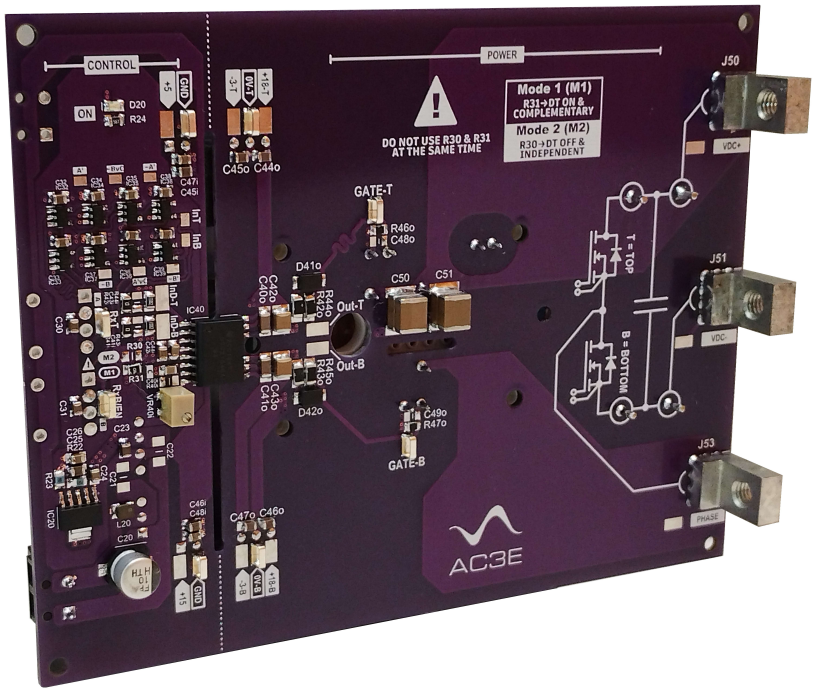


Figura 14: Convertidor AC3E.

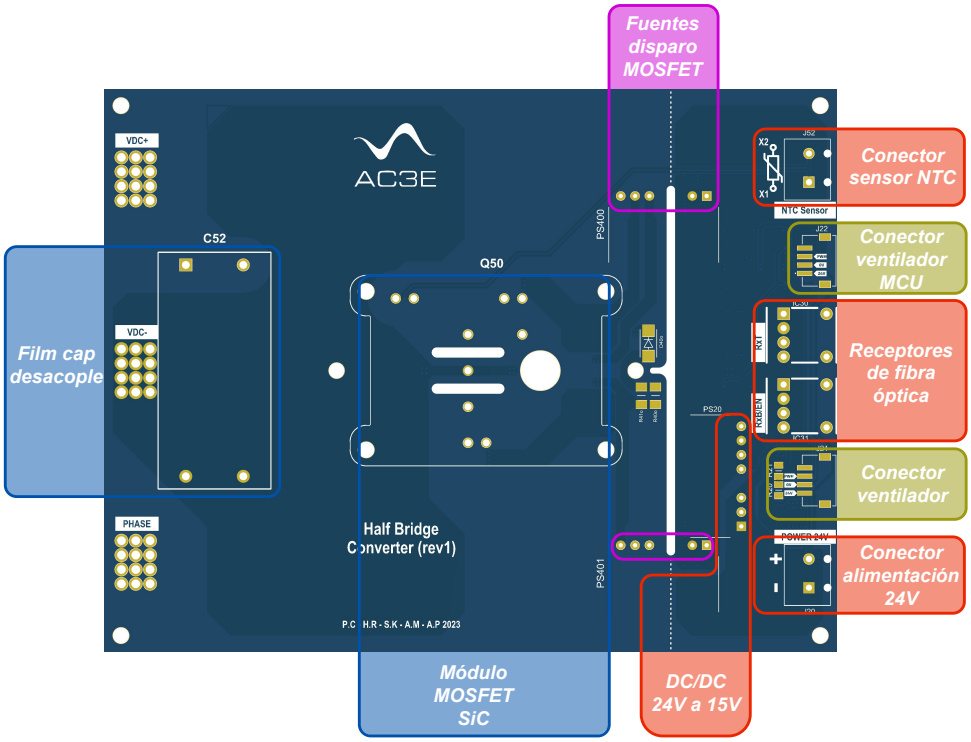


Figura 15: Vista superior.

La Fig.15 muestra la cara superior de la placa; en la disposición de esta versión todos los conectores externos y fuentes de la etapa de control se encuentran disponibles desde esta vista. También el módulo de MOSFET SiC se encuentra disponible desde este lado del inversor con la finalidad de que pueda montarse sobre el un disipador de las dimensiones de la placa (**100x130**).

Algunos detalles mecánicos de la placa que es importante mencionar es que los cortes que posee en la zona de montaje de los semiconductores cumplen la función de mejorar la aislación entre las señales de potencia (**+VDC, PHASE Y -VDC**).

La mayor parte de los componentes en esta vista son through hole; los únicos componentes de montaje superficial son los correspondientes al bootstrapping, que se encuentran a la derecha del módulo semiconductor, y los conectores para el uso de un ventilador externo.

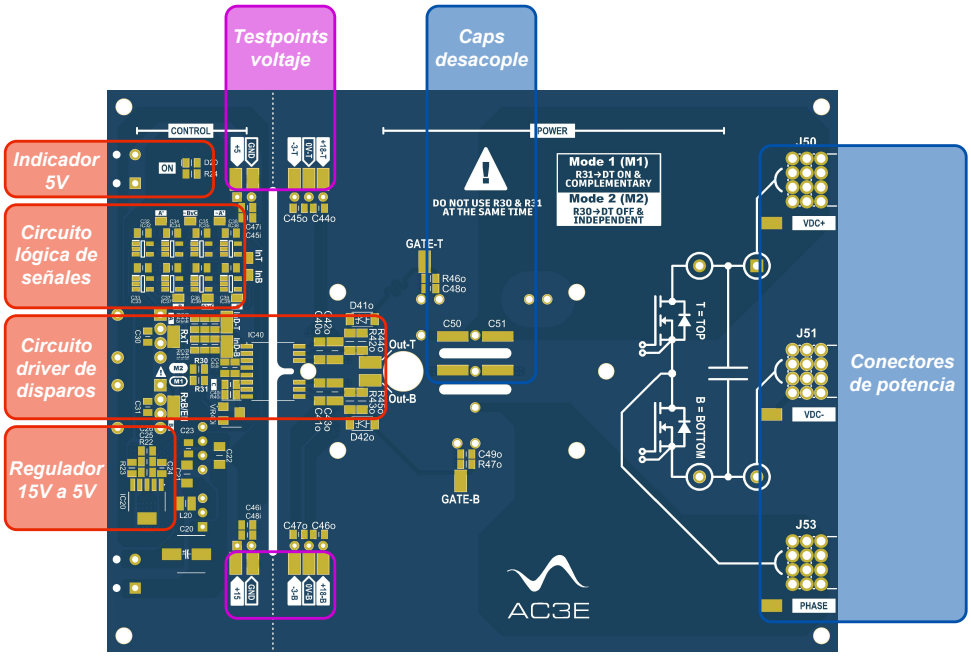


Figura 16: Vista inferior.

En la cara opuesta se encuentran montados todos los componentes que son de montaje superficial correspondientes a las etapas de control y potencia y también los conectores de potencia para un backplane como se ve en la Fig.16. Estos conectores se encuentran por este lado debido a que mecánicamente al ubicarse desde la capa mostrada en la Fig.15 provocarían una colisión con el disipador.

Se encuentran detalladas en la ilustración la concordancia entre la etapa y la zona de la placa utilizada. Al igual que en la zona de potencia, se encuentra un corte en la placa que divide las etapas de control de la de potencia justo en el sector donde se encuentra montado el driver optoacoplador y las fuentes asimétricas, de manera de mejorar la aislación.

5. Resultados experimentales

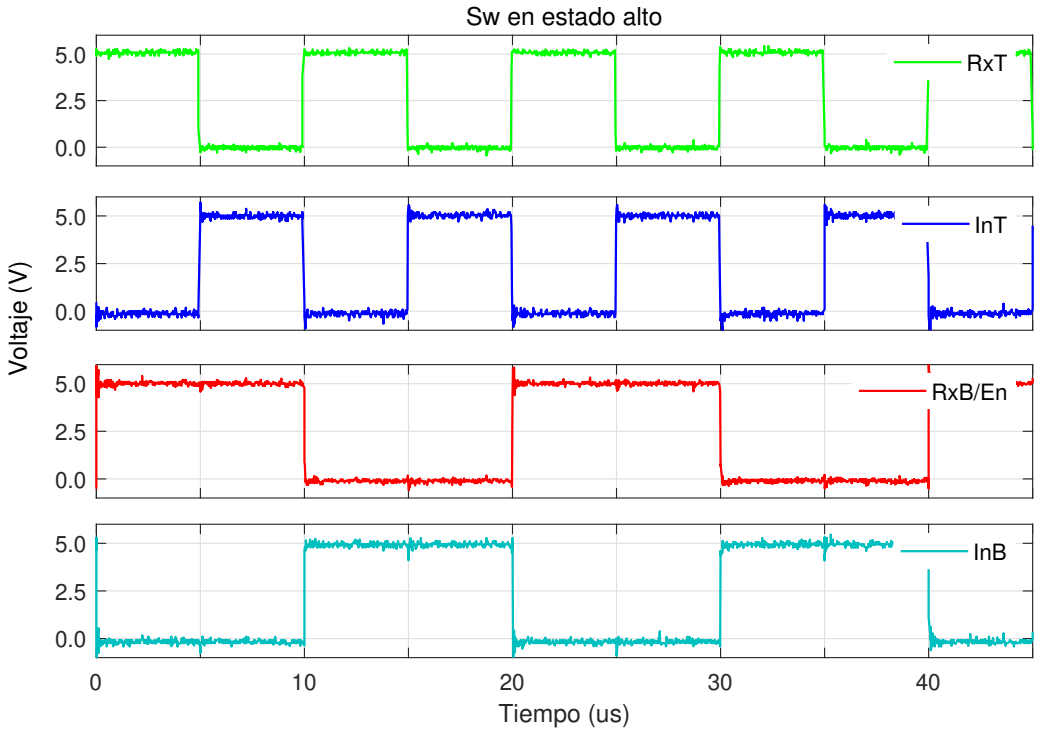


Figura 17: Validación de señales con Sw en estado alto.

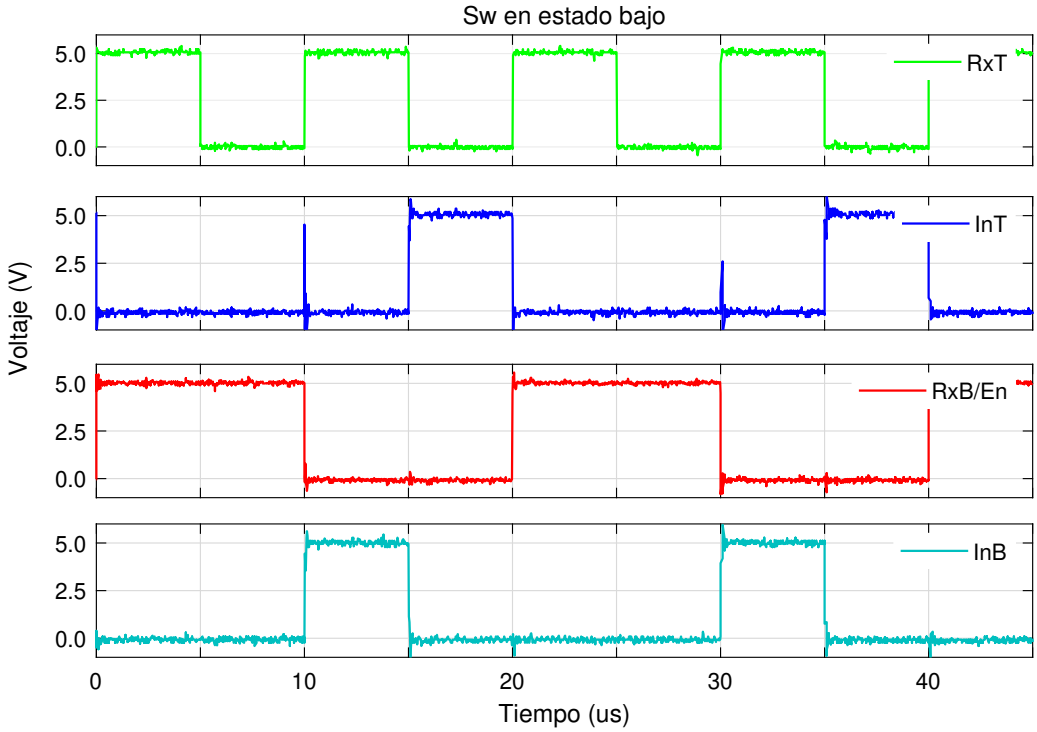


Figura 18: Validación de señales con Sw en estado bajo.

Las figuras recién presentadas corresponden a las validaciones experimentales de los circuitos propuestos anteriormente en las simulaciones. Estas pruebas se realizaron a una frecuencia de entrada de **100kHz** y **5V** proporcionada por un generador de señales. Para el caso en que se utilice $R30$, correspondiente a la señal Sw en estado alto, en donde el driver funciona en forma independiente y sin tiempo muerto, las señales obtenidas son las que se muestran en la Fig.17.

En el caso de que se utilice $R31$, que corresponde a Sw en estado bajo, en donde el driver estará implementando la función de tiempo muerto en operación complementaria a la señal de entrada se obtienen las señales mostradas en la Fig.18.

Para la señal de potencia de los semiconductores se realizaron un par de pruebas para evaluar la efectividad de un capacitor de película en la disminución del ringing de la conmutación. Las pruebas se realizaron con $100V$ y $150V$, y lo resultados se pueden observar en las Fig.19 y Fig.20.

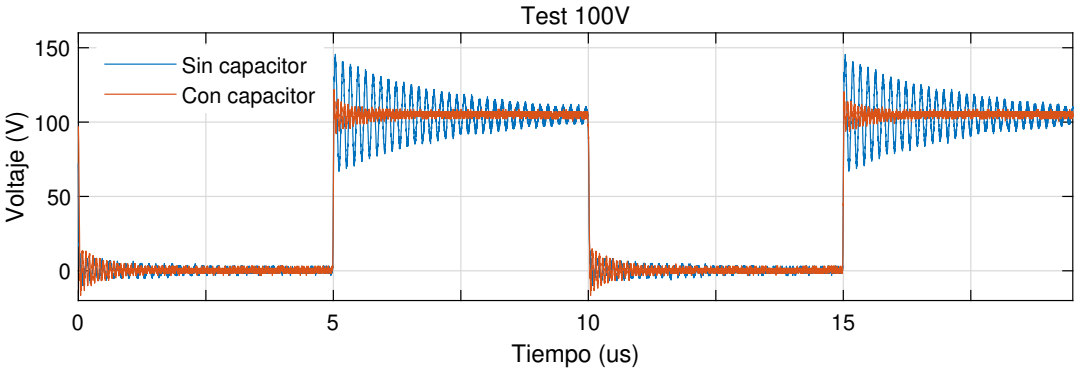


Figura 19: Conmutación a voltaje de 100V con film capacitor.

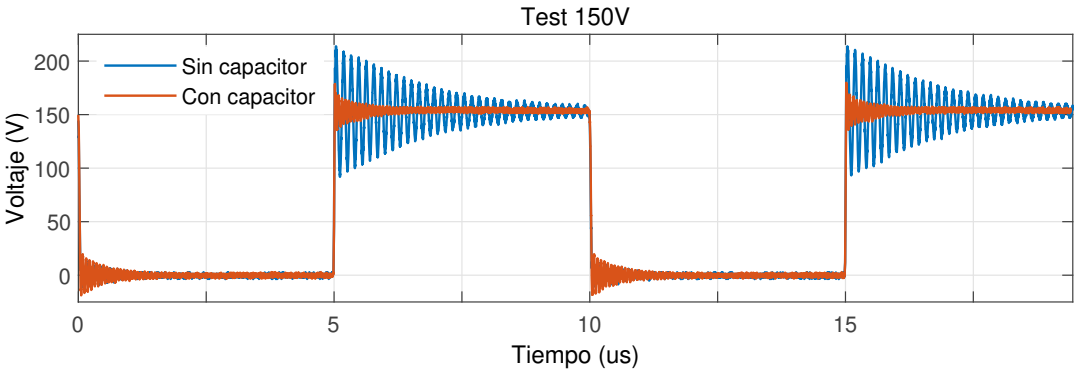


Figura 20: Conmutación a voltaje de 150V con film capacitor.

Se observa que el capacitor de desacople efectivamente reduce una gran cantidad de la oscilación causada por la conmutación. Eventualmente la respuesta podría mejorar dependiendo de la frecuencia que se utilice para dimensionar correctamente el valor del capacitor.

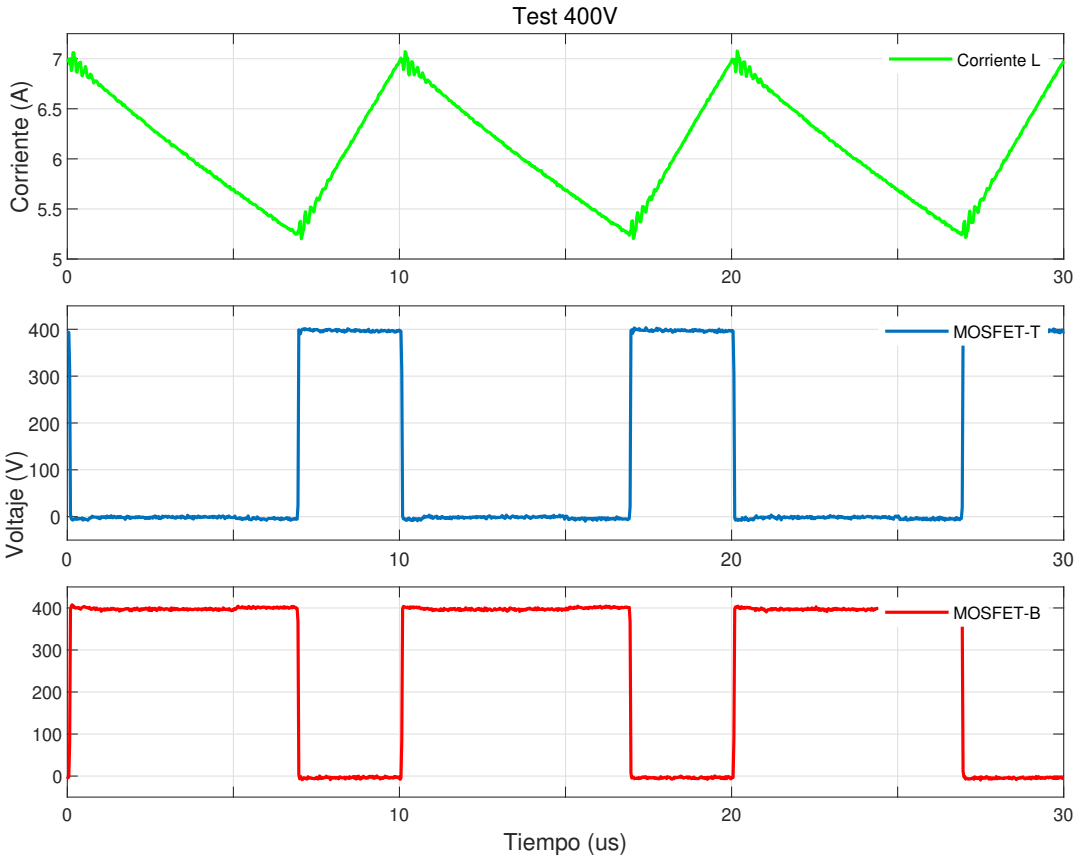


Figura 21: Prueba de Buck converter a 400V.

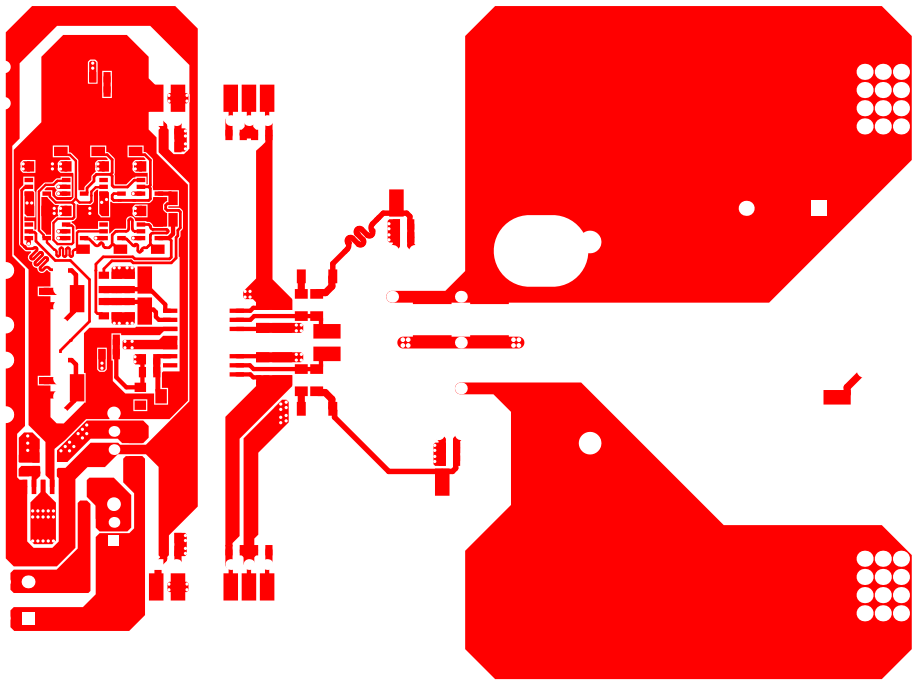
La Fig.21 muestra las mediciones de voltaje de conmutación de los semiconductores y la corriente a través del inductor de un convertidor Buck armado con la placa diseñada. La prueba se realizó a una frecuencia de **100kHz**, un voltaje de DC-Link de **400V** y un ciclo de trabajo del **30 %**.

6. Recomendaciones fabricación

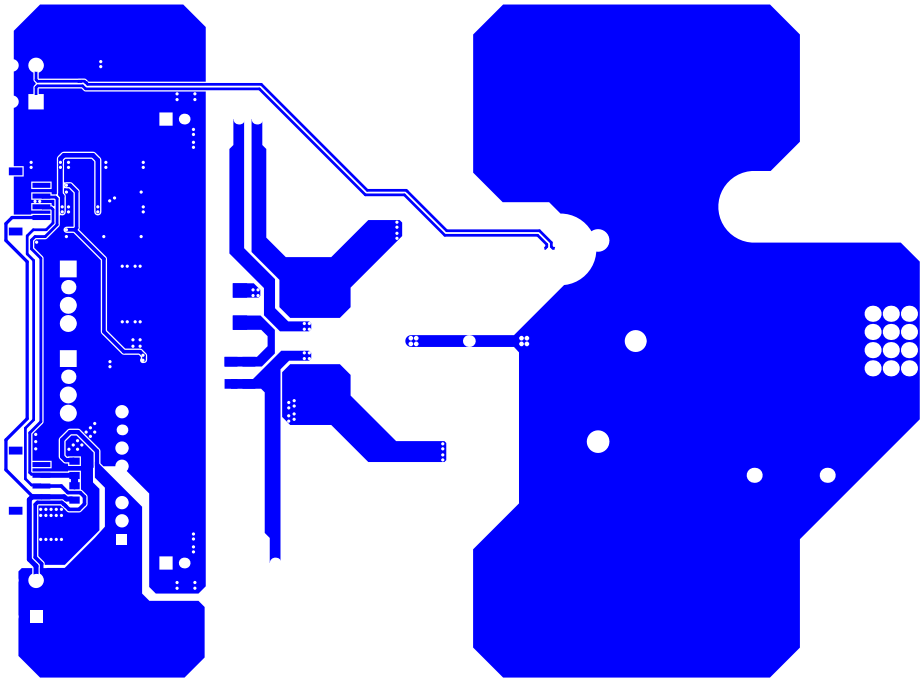
Se recomienda tener en consideración los siguientes parametros para la fabricación:

- Size: 100 x 130 mm
- Layer: 2 Layers
- Thickness: 1.6 mm
- Min hole size: 0.3 mm
- Via process: Tenting vias
- Material: FR-4: TG150
- Min track/spacing: 6/6mil
- Finished copper: 1 oz Cu

7. Anexos



Capa inferior placa inversor.



Capa superior placa inversor.

Appendix B

Thermal and electrical simulation schematic

The thermal and electrical simulation used in this thesis is presented. Closed loop control schemes described are in the PWM and PSM control subsystems. The Load Sweep subsystem changes the value of the variable resistors connected as loads of the converter every 0.75 simulation seconds, starting in 80Ω and diminishing 5Ω every step.

To assess the thermal losses of the semiconductors, manufacturers' thermal models were utilized. The efficiency of the converter was calculated using the Switch Loss Calculator block. This works by selecting the semiconductors under study and selecting the type of losses to be calculated. Afterwards, the Efficiency Calculator block uses the following equation to calculate efficiency:

$$\eta = \left(1 - \frac{P_{loss}}{P_{in}}\right) \cdot 100 \tag{B.1}$$

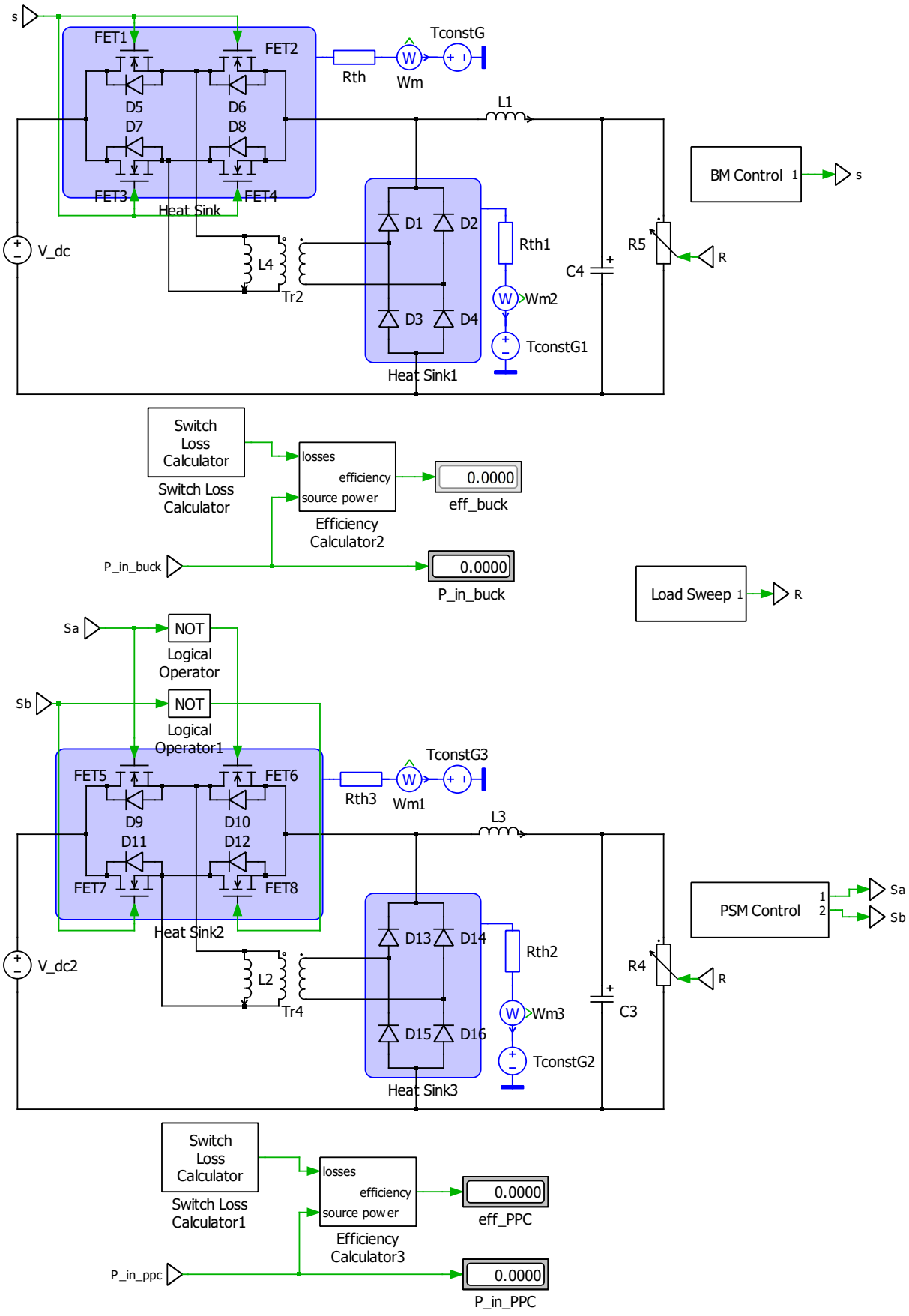


Figure B.1: Thermal and electrical simulation schematic

Appendix C

Generated Publications

C.1 International Conferences

[1] F. Gonzalez-Tijerino, H. Renaudineau, M. Perez, T.A. Meynard, S. Kouro, J. Rodriguez, "Modulation of Step-Down Partial Power Converter" , in IECON Madrid 2025, 2025.

[2] H. Renaudineau, N. Muller, D. Ulloa, F. Gonzalez-Tijerino, J. Rodriguez, "Partial Power DC-DC Converter Interface for Second-Life Battery with Signal Injection for Online Battery Monitoring" , in CHILECON 2025, 2025.

[3] S. Arenas-Perez, P.S. Canales, H. Renaudineau, J.W. Zapata, F. Gonzalez-Tijerino, C.A. Rojas, S. Kouro, J. Rodriguez, "Evaluation of Loss Modeling and Efficiency Estimation of SiC-based Half-Bridge Rapid Prototyping Platform" , in CHILECON 2025, 2025

C.2 Associated Projects

[1] This research was funded by ANID/Fondecyt Iniciacion/11240917, by AC3E (ANID/Basal/AFB240002), and by SERC Chile (ANID/FONDAP/1523A0006).

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[3] J. W. Zapata, S. Kouro, G. Carrasco, H. Renaudineau, and T. A. Meynard, "Analysis of partial power dc–dc converters for two-stage photovoltaic systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 591–603, 2019.

[4] H. Renaudineau, A. M. Llor, R. Cortés D., C. A. Rojas, C. Restrepo, and S. Kouro, "Photovoltaic green hydrogen challenges and opportunities: A power electronics perspective," *IEEE Industrial Electronics Magazine*, vol. 16, no. 1, pp. 31–41, 2022.

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